Honeywell

Process Management
Systems Division

GENERAL DESCRIPTION

4500 PROCESS COMPUTERS

TABLE OF CONTENTS

SECTION		PAGE
1	**INTRODUCTION**	1
1.1	MAJOR FEATURES OF THE TDC 4500 PROCESS CONTROL SYSTEM	1
1.2	SCOPE OF THIS GENERAL DESCRIPTION	3
1.3	REFERENCES	3
1.4	IMPROVED 4500	4
2	**SOFTWARE**	5
2.1	RTMOS	5
2.2	FREETIME IV	6
2.3	DEACON/CIA	6
2.4	FILES IV SYSTEM	6
2.5	OPO	6
2.6	TASC	6
2.7	PRODUCT SYSTEMS	7
2.7.1	SEER	7
2.7.2	SCADA	7
2.7.3	TDC PM/C	7
2.8	VIEW	7
3	**GENERAL INFORMATION**	9
3.1	ENVIRONMENTAL SPECIFICATION	9
3.2	INPUT POWER	9
3.2.1	System Cabinets	9
3.2.2	Memory Battery Backup Option	9
3.2.3	Peripheral Devices	9
3.2.4	Bulk Memory Units	9
3.3	CONSTRUCTION AND MODULARITY	9
3.3.1	Cabinets	9
3.3.2	Printed Wire Boards	10
3.3.3	Modularity	10
3.3.4	Maintainability	10
4	**CENTRAL SYSTEM UNIT**	11
4.1	PROGRAMMABLE ARITHMETIC UNIT	11
4.1.1	Instructions	11
4.1.2	Principal Registers, Counters, and Indicators	12
4.1.3	Main Memory Addressing	13
4.1.4	Arithmetic Operations	15
4.1.5	Arithmetic Data Formats	15

SECTION PAGE

4.1.6 Logical, Bit Manipulation, Field, Byte and Shifting Operations. . . . 16
4.1.7 Subroutine Linkage . . . 17
4.1.8 Circular Lists . . . 17
4.1.9 TIM/TOM Feature. . . . 18
4.1.10 Timekeeping. . . . 19
4.1.11 Stall Alarm. . . . 19
4.1.12 Memory Protect Option . . . 19
4.1.13 Interrupt Watchdog . . . 21
4.1.14 Programming and Maintenance Console . . . 21
4.1.15 Using the Console . . . 23
4.1.16 Timer Alarm Package . . . 24
4.1.17 Traps . . . 24
4.2 MOS MEMORY . . . 25
4.2.1 Error Detection and Correction . . . 26
4.3 AUTOMATIC PROGRAM INTERRUPTS . . . 26
4.3.1 Interrupt Addresses and Priorities. . . . 27
4.3.2 Interrupt Types. . . . 27
4.3.3 Inhibiting and Masking API's . . . 28
4.4 FIRMWARE FLOATING POINT OPTION. . . . 28
4.5 GENIE I/O CONTROLLER AND BUS . . . 29
4.5.1 I/O Controller Complement. . . . 29
4.5.2 GENIE I/O Bus GEN 2 Instructions . . . 31
4.5.3 Transfer Sequence - To and From AU . . . 32
4.5.4 Transfer Sequence - Direct To and From Main Memory . . . 33
4.5.5 GENIE I/O Bus Error Detection. . . . 34
4.5.6 Bus Extension and Switching. . . . 35
4.6 POWER FAIL RESTART. . . . 36
4.7 CSU POWER SYSTEM. . . . 36
4.7.1 MOS Memory Battery Backup Chassis. . . . 36

5 DRUM MEMORY . . . 39
5.1 FUNCTIONAL DESCRIPTION . . . 39
5.2 OPTIONS . . . 39
5.2.1 Drum Memory Unit Controller Options. . . . 39
5.2.2 Drum Options. . . . 39
5.3 PRINCIPAL FEATURES . . . 41
5.3.1 Latency Time. . . . 41
5.3.2 Start-Up Time. . . . 41
5.3.3 Accuracy. . . . 41
5.3.4 Transfer Rate . . . 41
5.3.5 Write Protection . . . 41

SECTION PAGE

5.3.6 Transferred Data Validity Verification. . . . 41
5.3.7 Power Failure Protection 42
5.4 OPERATING SEQUENCE 42
5.4.1 Transfer Sequence 42
5.4.2 GEN 2 Instructions 42
5.4.3 Automatic Program Interrupts 43
5.4.4 Alarm Detection 43
5.5 ADDITIONAL DRUM SUBSYSTEM CHARACTERISTICS 44
5.5.1 Primary Drum Cabinet Power 44
5.5.2 Drum Cabinet Physical Characteristics. . . . 44
5.5.3 Environmental Classes 44

6 MOVING HEAD DISC SUBSYSTEM 45
6.1 FUNCTIONAL DESCRIPTION 45
6.2 OPTIONS 45
6.3 PRINCIPAL FEATURES 46
6.3.1 Latency Time 46
6.3.2 Start-Up Time. . . . 46
6.3.3 Transfer Rate/Size 47
6.3.4 Write Protection 47
6.3.5 Data Validity and Recovery Techniques. . . . 47
6.3.6 Power Fail/Auto Restart. . . . 47
6.3.7 Head and Sector Optimization 47
6.4 OPERATING SEQUENCE 48
6.4.1 BMC Setup. . . . 49
6.4.2 Data Transfer Operations 49
6.4.3 Header Transfer Operations. . . . 53
6.4.4 Control and Test Operations 53
6.4.5 Termination Codes 55
6.4.6 Alarms/Error Detections. . . . 55
6.4.7 Command Descriptions. . . . 57
6.4.8 BMC Interrupts. . . . 58
6.5 ADDITIONAL CHARACTERISTICS 58
6.5.1 Disc Unit Primary Power. . . . 58
6.5.2 Disc Unit Physical Characteristics 58
6.5.3 Environmental Classes 58

7 MODULAR FURNITURE 59

8 PERIPHERAL DEVICES 61
8.1 PRIMARY POWER 61
8.2 TermiNet PRINTERS. . . . 61

SECTION PAGE

8.2.1 TermiNet Printer Options 62
8.2.2 Operating Features 63
8.2.3 Message Formats 63
8.2.4 Additional Features 64
8.3 LINE PRINTER 65
8.3.1 Operating Features 65
8.3.2 Printing Sequence 66
8.3.3 Additional Features 66
8.4 PAPER TAPE PUNCH 66
8.4.1 Operating Features 66
8.4.2 Record Format 66
8.4.3 Additional Features 67
8.5 PAPER TAPE READER 68
8.5.1 Operating Features 68
8.5.2 Record Format 68
8.5.3 Additional Features 69
8.6 CARD PUNCH 69
8.6.1 Operating Features 69
8.6.2 Card Punching Sequence 69
8.6.3 Additional Features 71
8.7 CARD READER 71
8.7.1 Operating Features 71
8.7.2 Card Reading Sequence 71
8.7.3 Additional Features 71
8.8 Matrix Printer Device 72.1
8.8.1 Matrix Printer Options 72.1
8.8.2 Matrix Printer Features 72.1
8.8.3 Operating Features 72.2
8.8.4 Message Formats 72.5
8.8.5 Additional Features 72.6

9 HONEYWELL PROCESS VIDEO (HPV-2) DISPLAY SUBSYSTEM 73
9.1 OPTIONS 73
9.1.1 Display Generator Options 73
9.1.2 Display Monitors 75
9.1.3 Keyboards 75
9.1.4 Light Pen Option 76
9.2 OPERATIONAL FEATURES 76
9.2.1 Alphanumeric Channel Set 77
9.2.2 Data Trend Channel Set 77
9.2.3 Video Display 78
9.3 COMPUTER/DISPLAY GENERATOR MESSAGES 79

SECTION PAGE

9.4 ADDITIONAL FEATURES 79
9.4.1 Physical Characteristics. 79
9.4.2 Power Requirements 79
9.4.3 Environmental Classes 79
9.4.4 Display Generator Interface. 79

10 HPV-1 HONEYWELL PROCESS VIDEO SUBSYSTEM 81
10.1 OPTIONS 81
10.1.1 Terminal Options 81
10.1.2 GENIE Interface Options 82
10.2 OPERATIONAL FEATURES 82
10.2.1 Editing Controls 82
10.2.2 Operating Modes. 82
10.3 ADDITIONAL FEATURES 82
10.3.1 Tagged Fields 82
10.4 STANDARD SOFTWARE 83
10.4.1 RTMOS. 83
10.4.2 FILES IV. 83
10.5 COMPUTER/DISPLAY GENERATOR MESSAGES 83
10.6 OTHER CHARACTERISTICS. 83
10.6.1 Desk-Top Terminal 83
10.6.2 Modular Components. 84

11 DIGITAL PROCESS INTERFACE SUBSYSTEM 85
11.1 FUNCTIONAL DESCRIPTION 85
11.1.1 Radial Port Configuration 85
11.1.2 Termination Assemblies and Interface Modules 85
11.1.3 Transfer Rates 87
11.2 DPI SUBSYSTEM OPTIONS. 87
11.2.1 Input Modules 87
11.2.2 Output Modules 88
11.2.3 Operator's Console Modules 88
11.2.4 Power Supplies 88
11.2.5 Termination Assemblies 89
11.2.6 Terminator Modules. 89
11.2.7 Termination Cabinets. 89
11.3 PROCESS INTERFACE MODULES. 89
11.3.1 Input Modules 89
11.3.2 Output Modules 91
11.3.3 Operator's Console Modules 94
11.4 DPI SUBSYSTEM OPERATING SEQUENCE. 94
11.4.1 Interrupt Scanning. 94

SECTION PAGE

11.4.2 Command, Data, and Status Exchanges . . . 95
11.4.3 DPI Subsystem Instructions . . . 95
11.4.4 Test Mode . . . 97
11.5 ADDITIONAL FEATURES . . . 97
11.6 SMALL DIGITAL I/O SUBSYSTEM . . . 97
11.6.1 Features . . . 98
11.6.2 Capacity . . . 98

12 ANALOG INPUT SUBSYSTEM . . . 99
12.1 FUNCTIONAL DESCRIPTION . . . 99
12.1.1 Local/Remote Controller Communication . . . 99
12.1.2 Analog Input Scanning . . . 99
12.1.3 Analog Input Parameters . . . 101
12.2 AIS OPTIONS . . . 101
12.2.1 Analog Input Termination Cabinets . . . 101
12.2.2 Termination Assemblies . . . 101
12.2.3 Analog Input Amplifier . . . 102
12.2.4 Signal Conditioning . . . 102
12.2.5 Thermocouple Inputs . . . 102
12.3 OPERATING SEQUENCE . . . 103
12.3.1 AIS Instructions . . . 103
12.4 ADDITIONAL FEATURES . . . 104

13 REMOTE COMMUNICATIONS . . . 105
13.1 ASYNCHRONOUS COMMUNICATION DRIVE . . . 105
13.1.1 Data Format . . . 105
13.1.2 Timing . . . 105
13.1.3 Received Character Recognition . . . 106
13.1.4 Current Loop . . . 106
13.1.5 Automatic Answering . . . 106
13.1.6 Line Turnaround . . . 106
13.1.7 ACD Instructions . . . 106
13.1.8 Additional Features . . . 107
13.2 DATA HIWAY INTERFACE (DHI) . . . 107
13.2.1 Data Formats . . . 107
13.2.2 Modes of Operation . . . 110
13.2.3 Computer Instructions . . . 111
13.2.4 Error Checks . . . 114
13.2.5 Options and Features . . . 114
13.3 PARALLEL DATA LINK . . . 115
13.3.1 Data Format . . . 115
13.3.2 PDL Instructions . . . 115
13.3.3 Additional Features . . . 115

SECTION PAGE

13.4 TRANSPARENT SYNCHRONOUS DATA LINK 115
13.4.1 TSDL Interfaces 115
13.4.2 Data Format 116
13.4.3 Character Recognition 117
13.4.4 Message Validity Verification 118
13.4.5 TSDL Instructions 119
13.4.6 Interrupts 121
13.4.7 Automatic Answering 121
13.4.8 Line Turnaround 121
13.4.9 Operating Sequences 121
13.4.10 Additional Features 122
13.5 HS7024 COMMUNICATIONS COUPLER 122
13.5.1 HCC Interfaces 122
13.5.2 Command and Data Formats 123
13.5.3 Message Validity Verification 123
13.5.4 HCC Instructions 126
13.5.5 HCC Interrupt 129
13.5.6 Line Turnaround 129
13.5.7 Additional Features 129

14 AUXILIARY SYSTEM CABINETS 131
AUXILIARY EXPANSION CABINETS 131
VIDEO EXPANSION CABINETS 131
ASSOCIATED OPTIONS 132

15 FLOPPY DISC SUBSYSTEM 133
15.1 DESCRIPTION 133
15.1.1 Disc Drive Units 133
15.1.2 Diskettes 133
15.2 OPTIONS 133
15.2.1 Model Numbers 133
15.3 FEATURES 134
15.3.1 Write Protection 134
15.3.2 Access Time 134
15.3.3 Validity and Error Checking 134
15.3.4 Recoverable Error Rate 134
15.3.5 Power Shutdown 134
15.3.6 Program Load 134
15.4 OPERATION 135
15.4.1 Setup 135
15.4.2 Transfer Sequence 136
15.4.3 Termination Status Codes 136

SECTION PAGE

15.4.4 GEN 2 Instructions . . . 136
15.5 OTHER CHARACTERISTICS . . . 138
15.5.1 Physical . . . 138
15.5.2 Power . . . 138
15.5.3 Environmental . . . 138

16 PORTED BULK MEMORY CONTROLLER AND BULK INTER-SYSTEM LINK . . . 139
16.1 FUNCTIONAL DESCRIPTION . . . 139
16.2 OPTIONS . . . 140
16.2.1 Model Numbers . . . 140
16.3 ADDITIONAL CHARACTERISTICS . . . 140
16.3.1 Power . . . 140
16.3.2 Ported BMC-CPU Interfaces . . . 140
16.3.3 Environmental Class . . . 140

17 MAGNETIC TAPE SUBSYSTEM . . . 141
17.1 FUNCTIONAL DESCRIPTION . . . 141
17.2 OPTIONS . . . 141
17.2.1 Bulk ISL Service . . . 141
17.3 OPERATING SEQUENCE . . . 145
17.4 CONTROL WORDS . . . 145
17.5 DATA FORMATS . . . 145
17.6 INSTRUCTIONS . . . 145
17.6.1 GEN 2 Instructions . . . 145
17.7 DATA PROTECTION . . . 150
17.8 TERMINATION STATUS . . . 150
17.9 CONTROLS AND INDICATORS . . . 152
17.10 MAG TAPE TRANSPORT AND FORMATTER CHARACTERISTICS . . . 153
17.10.1 Mag. Tape Transport . . . 153
17.10.2 Mag. Tape Formatter . . . 153
17.10.3 Environmental Class . . . 153

18 LARGE CORE STORE . . . 155
18.1 FUNCTIONAL DESCRIPTION . . . 155
18.2 OPTIONS . . . 155
18.2.1 LCS Controller Options . . . 155
18.2.2 LCS Options . . . 155
18.3 PRINCIPAL FEATURES . . . 156
18.3.1 Access Time . . . 156
18.3.2 Accuracy . . . 156
18.3.3 Transfer Rate . . . 156
18.3.4 Write Protection . . . 156
18.3.5 Transferred Data Validity Verification . . . 156

SECTION PAGE

18.3.6 Power Failure Protection 156
18.3.7 Multi-Access Controller Operation 156
18.4 OPERATING SEQUENCE 156
18.4.1 Transfer Sequence 156
18.4.2 GEN 2 Instructions 158
18.4.3 Automatic Program Interrupts 159
18.4.4 Alarm Detection 159
18.5 ADDITIONAL LCS SUBSYSTEM CHARACTERISTICS 160
18.5.1 Primary LCS Cabinet Power 160
18.5.2 LCS Cabinet Physical Characteristics 160
18.5.3 Environmental Classes 160

APPENDICES

A ANALOG INPUT SUBSYSTEM DEFINITION OF TERMS 161

B DIGITAL PROCESS INTERFACE (DPI) MODULES APPLICATION INFORMATION 163

C TDC 4500 COMPUTER SYSTEM INSTRUCTIONS 179

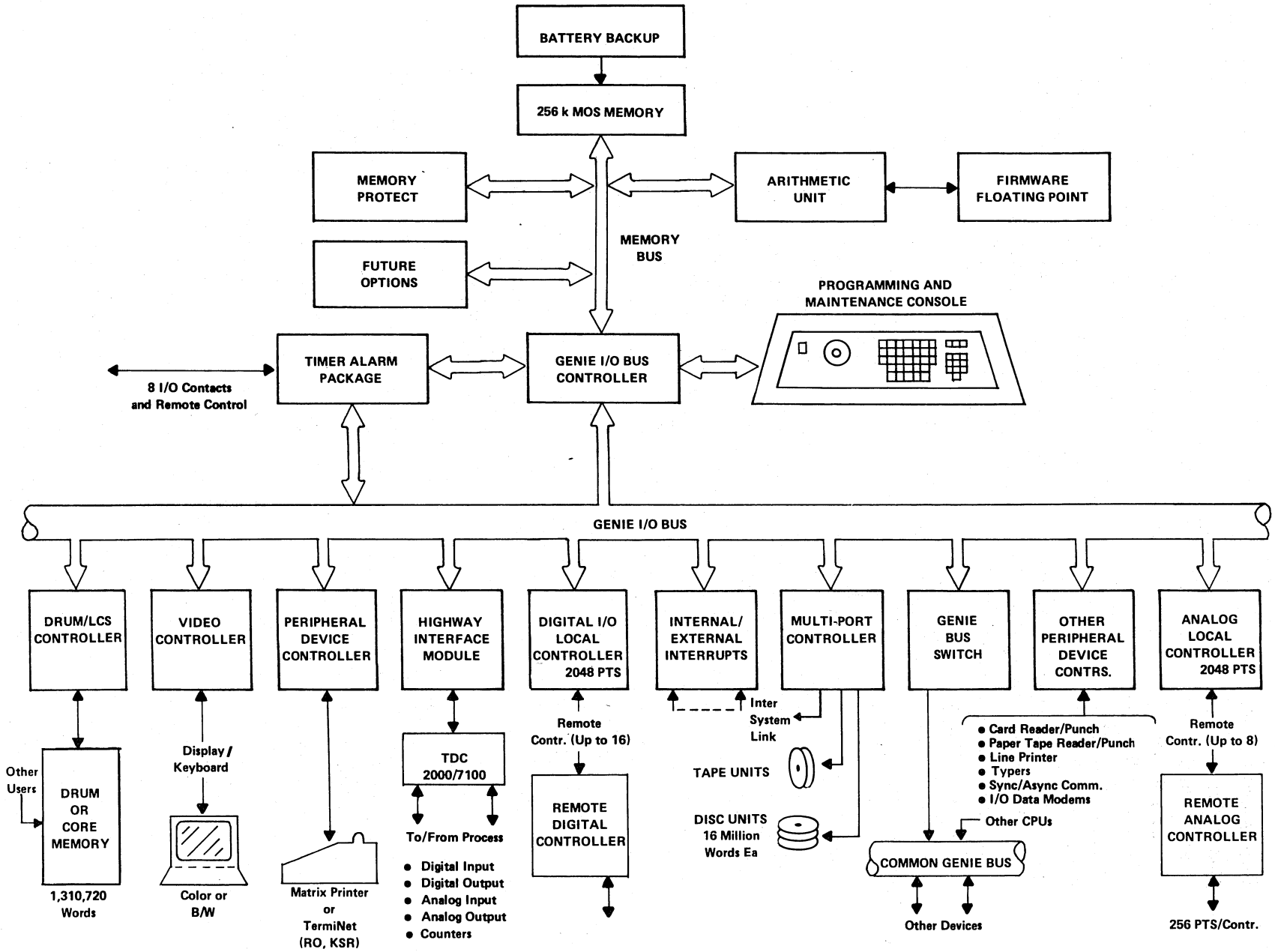

Fig. 1-1 TDC 4500

INTRODUCTION

This manual contains a functional description of the TDC 4500 process control computer system, manufactured by Honeywell Inc., Process Management Systems Division. The TDC 4500 is part of Honeywell's Total Distributed Control Architecture. All standard functional subsystems and options are described, including all pertinent parameters, speeds, capacities, data and instruction formats, and tolerances.

1.1 MAJOR FEATURES OF THE TDC 4500 PROCESS CONTROL SYSTEM

The TDC 4500 system is an upward extension of the Honeywell 4000 series process computer systems. Use of the Read Only Memory (ROM) and microprocessor concept have reduced the execution time of some instructions by as much as 75% over similar prior models. A block diagram of the system is provided on Fig. 1-1. While retaining the previous instruction set, major improvements and added features appear in the 4500 system which significantly improve performance and modularity, while reducing the physical size and cost of the equipment, as compared to earlier systems with similar capacity. Specifically, the 4500 system provides the following major features:

- Increased Memory Speed and Capacity

  Main memory cycle time is reduced to 600 nanoseconds, thereby accelerating instruction execution and improving throughput. The minimum 32 k Metal Oxide Semiconductor (MOS) memory may be expanded in the factory or in the field to up to 256 k (262,144) 24-bit words - four times more memory than in earlier systems. Provision has been made for possible future add-on options. Instructions and data read from the main MOS memory are guarded by an Error Detection and Correction (EDAC) feature which detects and corrects all single bit errors, detects all two bit errors and 90% of other multiple bit errors.

- Single Central System Unit Contains All Basic Control Functions

  The Central Processor and all basic peripheral and process I/O controllers are contained in a single 30" wide Central System Unit (CSU). See Fig. 1-2.

- Remote Intelligent Process I/O

  The CSU may be located up to 5000 cable feet from the Process Interface Units (PIU) which provide analog and digital connections to the process. This permits the CSU and peripherals to remain in a convenient central location. I/O data, parameters and instructions are exchanged between the CSU and up to 63 TDC 2000/7100 devices such as Operator Stations, Controllers or Process Interface Units over a single coaxial cable called the "data highway". The cost and complexity of connecting a CSU to the process is thereby significantly reduced.

  In addition to providing digital and analog I/O facilities, each PIU contains a microprocessor to monitor process operation. After being loaded with operating parameters, the PIU may be allowed to report on exception (i.e., limit or alarm conditions) thus taking a considerable burden off the CSU.

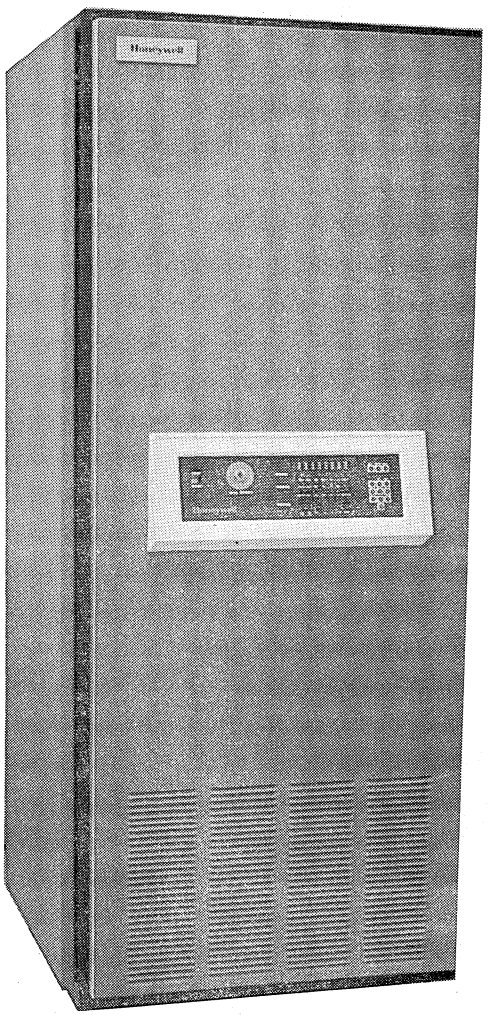

Fig. 1-2 Central System Unit

- Floating Point Option

  While floating point instructions are provided in the basic processor, faster instruction execution may be obtained with the firmware floating point option.

  The firmware floating point option provides medium speed performance single precision and most double precision floating point instructions. It is implemented by adding an additional set of ROM integrated circuits to a Central Processor board. The following floating point operations are provided: add, subtract, multiply, divide, fix, float and floating mode shift (d/p fix is always a quasi; floating mode shift is always a hardwired instruction).

- Modular I/O Packages

  The peripheral device controllers, process I/O controllers, and remote communication controllers are installed on the GENIE* I/O Bus for communication with the Central Processor under program control, via Table Input and Output Operation (TIM/TOM), or via Direct Memory Access (DMA). The fully modular I/O Bus concept permits the addition of any controller at any time by plugging the controller into an unused slot on the bus. Controller addresses and interrupt priorities are selected via option pins or switches on the controller modules. GENIE Bus chassis are provided or added to 4500 systems as required to accommodate the controller complement.

- Upward Program Compatibility

  The 4500 system retains the same instruction set used on 4400 and 4010 systems and is program compatible with those systems. New Byte and Field instructions have been added to simplify programming and increase performance. Most former software Quasi instructions and increased memory addressing capabilities have been implemented into Honeywell's line of proven software designed expressly for process control systems.

- Easy Expansion

  The modularity concept of the 4400 process computer is carried over to the 4500 and improved. Virtually all additions and expansions are accomplished merely by plugging in the new hardware and attaching interconnecting cables. The GENIE I/O Bus permits an almost unlimited variety of process I/O, remote communications, bulk memory, and peripheral device controllers to be implemented.

- Improved Man/Machine Interfaces

  The ease with which plant operating personnel can communicate with the process control system is important to the overall effectiveness of the system. The 4500 process control computer system offers two video display subsystems which provide excellent interaction with the control system. The video display subsystems provide either monochromatic or seven-color video displays of alphanumeric characters, symbols, and punctuation marks. In addition to the video displays, both standard and specially designed process operator's consoles are available. These subsystems and devices are capable of providing the operating personnel with a wide variety of information, and where appropriate, allow the entry of data and control commands into the computer system.

- Advanced Packaging - Modular Furniture

  The 4500 system is packaged using advanced packaging techniques which take advantage of state of the art electronics and integrated circuits. The system cabinets and optional modular furniture are appearance coordinated, and designed for ease of use and comfort for the operators. The modular furniture line provides an extensive variety of tables, desks, and consoles to accommodate the peripheral devices, video displays and keyboards, and process operator consoles.

- Maintainability and Product Support

  The design and packaging of the 4500 system contribute to its maintainability. The modular design of the system electronics permits quick and easy access to replaceable subassemblies. Test and diagnostic programs are supplied to verify the performance of each standard subsystem. Documentation provided with each system includes theory of operation publications; maintenance manuals with detailed performance testing, preventive maintenance, and troubleshooting procedures; PWB drawings; parts lists; this General Description; a Site Planning Manual; and Standard Software manuals. Training for customer personnel is available in both hardware maintenance and programming. An experienced Field Engineering force is ready to support the equipment on an "as needed" or contract maintenance basis. For additional details, refer to the 4500 Site Planning Manual.

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- Additional Features

  Many valuable features proven significant in previous 4000 series computers are included in the 4500 system. These include 24-bit word length, relative addressing, bit manipulation and testing, logical operations, TIM/TOM for tabular I/O operations that do not affect the AU registers, optional Memory Protection, and proven software.

  Some new features include Memory Battery Back-up option, an automatic rechargeable power system which preserves the contents of MOS memory for a minimum of 15 minutes after ac power failure; Auto Reboot, a feature which initiates reloading main memory from bulk storage if necessary following ac power failure, and a Timer Alarm Package.

  The Timer Alarm Package contains:

  1. A 2 kHz programmable clock with interrupts for high resolution timing.

  2. A hardware status monitoring system with contact outputs.

  3. Facilities for up to eight programmable output contacts and up to eight readable contact inputs.

  4. Two remote control inputs.

1.2 SCOPE OF THIS GENERAL DESCRIPTION

This document defines the 4500 process control system and its functional features. The features and performance of each standard subsystem available in the 4500 system are described. The actual contents of any individual 4500 system are described by the procurement documents for that system. Honeywell Inc. reserves the right to modify at any time without notice to customer the contents of this document or the design or functions of the system or any part thereof for reasons of improved performance and operational flexibility. If any conflicts exist between this General Description and Honeywell's applicable Functional Design Specifications, the latter will take precedence. In a given transaction between Honeywell and a customer, the provisions of the contract document will define Honeywell's obligation to the customer.

1.3 REFERENCES

This manual is intended as a general reference for hardware-oriented users, software-oriented users, and those concerned with the interrelationships between the hardware and software. Reference to other manuals and publications may be useful or necessary in understanding and using the 4500 functional subsystems described in this General Description. The publications and manuals referred to here are available from Publications, Process Control Division/ Phoenix.

Software publications include:

- RTMOS* (Real-Time Multiprogramming Operating System) Summary Manual, RTMOS Planning Manual, and RTMOS Application manual.

- Summary and Application manuals for software systems that run under RTMOS, including Deacon/CIA, FILES IV, and FREETIME IV.

  Similar manuals are available for other standard software subsystems.

- PAL (Process Assembly Language) and Process FORTRAN language manuals.

Other publications of interest to both software- and hardware-oriented users include:

- TDC 4500 Summary of Hardware Characteristics. A pocket folder listing all instructions alphabetically and by operation code. Specification summaries for the principal subsystems are also provided.

- Instruction Reference Manual. A more detailed description of the 4000 series instruction set than is provided in Appendix C to this General Description.

- Computer Operator Subsystem (COS) Manual. A manual for operators using COS, which runs under RTMOS, for program loading, memory changes, dumps, memory comparisons, placing devices or subsystem in or out of service, updating system data and time, etc.

While the theory of operation publications, which are provided in the documentation supplied with each shipped system, are primarily intended for the use of hardware maintenance personnel, they often are useful to Programmers, System Engineers, and Analysts in understanding

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some of the more intricate features of the subsystems they describe. It is intended that this General Description will describe all necessary machine level operating and programming details with no theoretical discussion, but in some cases, the meaning of those details can be better understood if the theory is known.

In addition to the Theory of Operation book sets provided with each shipped system, a Computer Maintenance Manual, and a System Drawings book set are provided. The theory, maintenance, and drawings book sets are made up to reflect the actual contents of each system.

Several references to the TDC 4500 System Configuration Guide and to some Engineering drawings appear in this General Description. These documents are available to Honeywell personnel as they are needed in determining specific system configuration details.

1.4 IMPROVED 4500

Early in 1979, slight production changes were made to improve the basic 4500. The principle feature of these changes is a redundant bulk memory bootstrap loader as described in part 4.1.15 and 4.6 of this document. Other minor differences are noted in this document where applicable. A kit is available to convert 4500A models to B models but this step may also require some system reconfiguration and should be planned with the help of a Honeywell representative.

SOFTWARE

One of the most important features of the TDC 4500 computer system is its line of standard software products. In order to provide assurance of a successful and efficient process computer system at minimum project cost, the hardware and software have been designed to complement each other. The standard software product line is extensive, is designed to minimize the amount of special programming required for individual process computer systems, and is under continuing expansion, as the technology grows. The software products which are offered with an individual system proposal are described in the proposal material.

The standard software products can be divided into two groups: 1) programs which run while the computer is on line and controlling the process, and 2) programs which may run while the computer is off line. All of the programs in the first group run under the control of RTMOS. Included in RTMOS are the process and peripheral input and output subsystems and memory protection subsystem. Program systems under the control of RTMOS include FREETIME IV, VIEW*, DEACON*/CIA, and the software for product systems such as SEER* and SCADA plus several other routines and subsystems necessary to the operation of the process computer system. The programs in the second group consist principally of assemblers, program loaders, printed and punched memory dumps, hardware test programs, and other operator communication and language processing products. Loaders, dumps, and operator communications packages are also available for use on line, as a part of, or under the control of RTMOS.

TDC 4500 computer system programs can be written in one or a combination of two languages: USASI standard FORTRAN IV and Process Assembler Language (PAL). FORTRAN is most useful for mathematical computations necessary in every process control system, especially in areas subject to change such as mathematical models and performance calculations. PAL offers maximum efficiency in the use of time and memory, especially in those areas of the program system pertaining to logical operations, housekeeping, and program control.

A large family of standard software products is available to minimize the time required to get the computer on line controlling the process. Additional programming for specific process applications can be easily combined with the standard software.

The standard software for the TDC 4500 provides process control through RTMOS and application programs in the foreground, and through FREETIME IV, it provides background processing and program development. RTMOS schedules and controls the programs in the family, handles the input and output of information, and oversees the performance of the computer hardware. Refer to the application and user manuals for these software systems to determine specific hardware configurations necessary to support them.

2.1 RTMOS

All of the TDC 4500 on-line programs operate under control of the Real-Time Multiprogramming Operating System (RTMOS). RTMOS is the most powerful process control operating system available. It is designed to meet the requirements of the total process environment. RTMOS is field proven in a variety of applications and it has won a reputation unequaled by any other operating system in the industry.

RTMOS is a software system which supervises program interaction with process events, time, the computer peripherals, and the central processing area of the CSU. RTMOS takes care of code conversion, peripheral device status monitoring, interrupt response, memory allocation, and many other functions.

RTMOS determines the mixture of programs to have in main memory, and which of these to execute on the basis of time, events, and priorities. A high load factor on all system resources is attained because the hardware is not left waiting while some other function is being performed.

RTMOS is a true multiprogramming operating system. It allows several programs to be active simultaneously. A program, once started by RTMOS, runs until it is interrupted, completed, or until it delays itself.

If the highest priority program that needs to run is not in main memory, RTMOS finds space there, and transfers the program from bulk memory. If a lower priority program is in main memory, and is asking to run, RTMOS runs that program while the bulk transfer is taking place. The relative addressing hardware permits the location of the programs in any available memory space.

If a program must be interrupted, RTMOS reloads the program from bulk memory if necessary, when it can be run again. It restores registers and intermediate data, and the program continues where it left off.

A Computer Operator Subsystem package is provided with RTMOS which allows access to memory through an input/output typer. This package permits on-line memory

*Trademark

changes, media conversions, dumps onto the typer, cards, or tape, and changes to several system functions.

2.2 FREETIME IV

FREETIME IV allows program debugging and development on the 4500 computer while it is on line and controlling the process. It makes use of the frequent relatively short intervals, when the computer system is not involved in active process monitoring and control.

FREETIME IV permits a faster system start-up by allowing a portion of the process control system to be on line while other portions are being debugged.

Programming costs are reduced through the use of FREETIME IV because:

- FREETIME IV diagnostic aids permit faster debugging.
- Full USASI Standard FORTRAN is available, making faster program writing possible.

2.3 DEACON/CIA

DEACON (DElineator And CONtrol) is an off-line debugging program designed to aid the programmer by allowing him to examine or change the contents of registers or memory locations. DEACON can be instructed to search memory for locations containing values which are equal to, not equal to, greater than or less than a certain number. It can trap illegal instructions and monitor for specified conditions Input to DEACON may be in any of five formats including octal, ASCII, or binary.

CIA (Core Image Analyzer) also a debugging program, may be used to print the contents of one or many memory locations, search working or bulk memory for locations containing values which are equal to, less than, greater than, (or the converse thereof) a specified value. CIA can search memory for bit patterns and compare the contents of working memory with bulk memory.

Both DEACON and CIA run under RTMOS and need at least one typer to operate. While not required, a line printer is desirable for long memory dumps.

2.4 FILES IV* SYSTEM

FILES IV is a software system designed primarily to facilitate creation and easy modification of source programs, data and other files from CRT terminals. Other features of the system include:

- Interface to FREETIME IV capabilities (i.e., source programs can be compiled from a file, rather than cards)
- Media-to-media file transfers and file maintenance
- File backup to other media
- File access by using callable resident subroutines

The FILES IV system operates as a background function in the real-time process control environment and will run at a priority level defined for the specific system. At its lowest priority level assignment, the system will only have access to CPU time not essential to the process control system running in the foreground.

2.5 OPO

OPO optimizes process operation. It uses a customer generated mathematical model of the process to adjust the values which represent process conditions and materials, such that the optimum use of such material is made and the process objectives are maximized.

The mathematical model of the process is written in FORTRAN. In many applications, it can be written by the process control engineer, who may already know FORTRAN, or can learn it easily. The model is integrated into the OPO system by the user, and OPO may then provide on-line process optimization or may provide data pertaining to the results of a simulation of the process and its optimization.

2.6 TASC

Tabular Sequence Control (TASC) is a high-level, interpretive language that allows coding directly from symbol form, using the parameters of a process control flow chart. Several question, action, and breakpoint symbols are defined. Process input and output data can be given actual point ID's or can be given symbolic names. Process parameters are specified in decimal. Inherent in the TASC system is a structure for control system design incorporating the use of video, a dedicated pushbutton panel, and printed messages to the operator.

Scheduling and execution of the TASC programs are performed by the TASC Operating System. It functions in the environment of the SEER product system and relies upon SEER for scanning alarming and video functions.

*Trademark

2.7 PRODUCT SYSTEMS

It is common to think of computer systems, including computerized process automation systems, as consisting of two different but related products: hardware and software. A significant feature of Honeywell Process Control Division/ Phoenix's products is that they are not separate hardware and software, but are fully integrated product systems, consisting of hardware, general purpose software, and application software, all combined into a product system package that can readily be applied to specific customer applications. The more prominent product systems are TDC PM/C, SEER, and SCADA. These are briefly described in the following paragraphs. Refer to the brochures and summary manuals on these and other product systems for further information.

2.7.1 SEER

SEER is a Steam Electric Evaluation and Recording system designed for electric utility steam stations. SEER scans hundreds of plant conditions, records the information, alerts operators to out-of-limits and alarm conditions, prints hourly and daily logs of plant conditions, and provides trends of variables as loads and other conditions change with time.

2.7.2 SCADA

SCADA is a Supervisory Control And Data Acquisition system that is applied to power distribution systems and to industrial processes. The data acquisition and control are accomplished through HS7024 Telecontrol Equipment Remote Stations which communicate with TDC 4500 process computer over voice grade lines. The Remote Stations are located at distant, typically unattended, remote sites such as power substations, remote generating units, gas transmission stations, pipeline stations, and water treatment plants. The SCADA system offers a powerful human interface subsystem that puts dispatchers and process operators right on top of the situation.

2.7.3 TDC PM/C

TDC Process Monitor and Control is a product system consisting of standard hardware and software that comprise a complete system that can be applied to virtually all industrial applications where process interface, operator interface, and data base management are required. TDC PM/C can be used as a data acquisition system only, a scan-log-alarm system, a supervisory control system, a direct digital control system, or any combination of these.

The basic TDC PM/C software, like all standard on-line software products, runs under RTMOS, and is preprogrammed to minimize the time and effort needed to get on-line. Its application to the process is defined by the customer and/or Honeywell through fill-in-the-blanks forms, through Honeywell's BICEPS Programming Language (BPL), through FORTRAN, or a combination of these procedures.

TDC PM/C systems can start quite small and be expanded as the process and PM/C's application to it grow. It can utilize our complete line of process interfaces and offers operator interfaces ranging from inexpensive black and white video consoles to seven-color video display consoles offering character-graphic schematic displays and alphanumeric tabular displays.

2.8 VIEW

VIEW is a video display software feature provided as part of SEER, SCADA, or AGC that facilitates the construction and modification of interactive video displays for process operator and engineer interfaces. VIEW allows process engineers to define the displays that provide process operators with a realistic view of the process and the computer's interaction with the process. The engineer builds or modifies the displays and defines the behavior of various display elements through English language statements entered through a video display and associated keyboard. Once a family of displays is built for a specific process application, VIEW's display generator produces the display, as requested, through the RTMOS video display interface software. Currently VIEW is supported by the HPV-2 (Honeywell Process Video) display system described elsewhere in this publication.

CONDITION	GENERAL INDUSTRIAL			OFFICE
	A	A1	A2	C
Operating Temperature Room Ambient	0°-50° C	0°-60° C	5°-40° C	18°-29° C
Cabinet - Internal	0°-70° C	0°-70° C	5°-60° C	18°-44° C
Relative Humidity (32° C Max. Wet Bulb)	5% - 95%	5% - 95%	5% - 95%	10% - 80%
Storage or Shipment Temperature	-35° to +70° C (all classes)			
Operating Altitude	to 7500 ft. (all classes)			
Shipping or Storage	to 35,000 ft. (all classes)			

Table 3-1 Environmental Classes

The information in this section applies to all TDC 4500 process computer system equipment unless specifically excepted in the remaining sections of this manual.

3.1 ENVIRONMENTAL SPECIFICATION

Detailed environmental specifications for the 4000 series of process computer systems are provided on drawing no. 68A974933, Equipment Environmental Specification. In that specification, the equipment is divided into two major classes, according to the intended environment for the equipment. The two classes and a summary of the principal environmental conditions for each class are indicated on Table 3.1.

The environmental class for each standard subsystem and device, and any exceptions to that class pertaining to the subsystem or device, are specified in the remaining sections of this General Description. The environmental statement for each device or subsystem will be found near the end of the description for each subsystem or device. A complete 4500 system is subject to the most restrictive environmental class of any of its devices or subsystems, unless the equipment subject to more restrictive environmental conditions can be enclosed or housed in an area conforming to its class, which is apart from the equipment in a less restrictive class. Normally, the CSU and all of its contents are in environmental class A. The process I/O termination cabinets, the Process Interface Units and the contents are usually rated for environmental class A1. Peripherals using paper media (cards, tape, etc.) must be maintained between 20 to 65% relative humidity. For additional information on the environmental classes, refer to the TDC 4500 Site Planning Manual.

3.2 INPUT POWER

3.2.1 System Cabinets

The Central System Unit (CSU), Auxiliary System Units (ASU), and process I/O termination cabinets require single phase 104 to 127 Vac power, supplied on three lines (high, neutral, and safety ground), at 47 to 63 Hz. 220 V, 50 Hz operation may be achieved by using a suitable transformer. The CSU power system is designed such that start-up current surges will not exceed three times the full load current value. See the TDC 4500 Site Planning Manual for input connection information and current requirements.

3.2.2 Memory Battery Backup Option

An optional Memory Battery Backup chassis is available to preserve the contents of MOS Memory in case of ac power failure. The MOS Memory is automatically switched to battery power during ac power outages. Battery power is sufficient to preserve the contents of a 256 k memory for at least 15 minutes. Battery output is monitored and power is automatically disconnected from memory if the voltage deteriorates below a safe level. An operator can determine whether memory power was lost by observing an indicator on the chassis. When ac power returns, the CSU firmware senses the battery condition to determine an appropriate start-up sequence. The batteries have an estimated four to five year life and are kept charged by a trickle charger.

3.2.3 Peripheral Devices

All peripheral devices, including typers, card readers, paper tape readers, card punches, paper tape punches, line printers, video display equipment, etc., plug into standard three-pin wall sockets (high, neutral, and safety ground) supplying 105 to 129 Vac. They are normally supplied from the same ac distribution system that supplies the CSU or ASU that controls them. See the TDC 4500 Site Planning Manual for input current requirements.

3.2.4 Bulk Memory Units

Drum Units are supplied via a three-wire (high, neutral, and safety ground) power cord with a plug. Input requirements are 105 to 129 Vac at 59 to 61 Hz or 217 to 253 Vac at 41 to 51 Hz. Refer to the TDC 4500 Site Planning Manual for input power requirements.

Disc Units require either single phase 102 - 132 Vac 60 Hz + .6, -1 Hz or 220 Vac 50 Hz power. Each unit requires 8.2 amps running current at 120 Vac.

Large Core Store Units are powered by 117 Vac, 47-63 Hz. Fully populated LCS units require 5 Amps maximum running current.

3.3 CONSTRUCTION AND MODULARITY

3.3.1 Cabinets

All of the electronic circuitry in the computer system, except for that contained in the peripheral devices, Drum

Unit, Disc Units, etc., is housed in heavy-duty cabinets, suitable for use in an industrial environment. Where necessary, the cabinets are cooled by blower-driven air. Air filters are installed in cabinets with blowers to remove dust and dirt from the air supply. The standard "30-inch" cabinet used in most applications is approximately 76 inches high, 30 inches wide and 32 inches deep. 19-inch mounting flanges are used to hold standard modular electronics chassis. Front and rear access is provided by magnetically latched doors. The top and side panels are removable. Cable access is normally through the bottom. 30-inch cabinets are used to house the CSU, AX or VX Expansion Cabinets, Shared memories and APIA/APID series process I/O termination electronics. TDC 7100 Process Interface Units (PIU) also use the standard 30-inch cabinet except for Low Energy units which use a NEMA 4 enclosure. TDC 2000 process I/O equipment mounts in 19-inch or 24-inch wide cabinets from 28 to 77 inches high. Refer to the TDC 4500 Site Planning Manual for additional information.

3.3.2 Printed Wire Boards

All electronic components, except for some components used in power supplies, are installed on plug-in printed wire boards. Integrated circuits are used almost exclusively. The integrated circuit complement includes small, medium, and large-scale (SSI, MSI, and LSI) units.

3.3.3 Modularity

The Central Processor and all basic system controllers are installed in a single Central System Unit as shown in Fig. 3-1. Larger systems, incorporating many I/O controllers and or devices, may require one or more Auxiliary System Cabinets to house additional modules that exceed the capacity of the CSU. All TDC 4500 system hardware is fully modular and can be implemented in the factory or in the field by plugging in and/or bolting on the necessary modules. The chassis are normally prewired to accommodate all optional modules at the maximum capacity. There may be cases where special wiring to accommodate a customer's particular requirements is provided, and a very few functional subsystem options are implemented by minor wiring changes. The vast majority of functional subsystem options are implemented by installing printed wire boards or by selecting jumper pin or switch configurations.

3.3.4 Maintainability

TDC 4500 process control computer systems are designed for maximum reliability and availability. The modularity of the system hardware contributes greatly to its maintainability. Modern construction techniques and circuitry reduce the physical size of the equipment and thereby minimize the degree of difficulty and time in locating suspected defective components. Several functional subsystems utilize built-in register and status displays and manual intervention controls to aid in troubleshooting. Special test aids are also available for some of the subsystems, and test and diagnostic programs are provided for all standard subsystems. The system documentation, which includes theory of operation manuals, detailed maintenance instructions, and necessary engineering drawings, is designed to minimize the degree of specialization required of maintenance personnel.

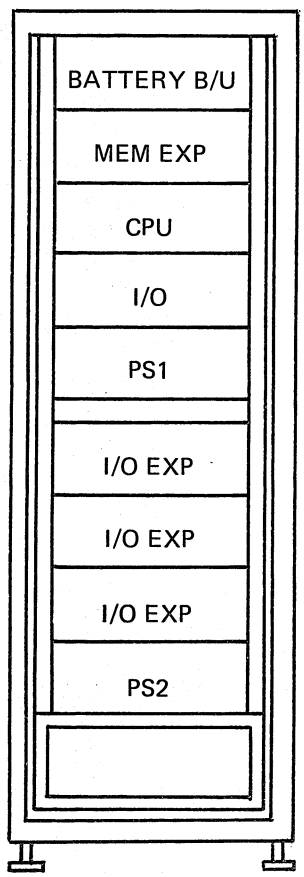


Fig. 3-1 TDC 4500 CPU With Major Options

CENTRAL SYSTEM UNIT

The Central System Unit (CSU) is the control, sequencing, and computational center of the TDC 4500 process control computer system. It contains all of the basic control modules in the system, including the Central Processor and the basic controllers for all standard functional subsystems. The Central Processor is the primary computational and control center and it consists of the Microprocessor-based Arithmetic and Logic Unit, the Memory Bus Controller, GENIE I/O Controller (which includes automatic program interrupt logic) and main memory. Supporting functions such as the Floating Point option, Program Load, Auto Reboot and Memory Protect may be considered as functions of the Central Processor. The Central Processor is often called the "processor" or "CPU".

Basic Central Processor Unit model ACPU11 includes the cabinet, Arithmetic Unit, GENIE I/O Controller, Programming and Maintenance Console, first Power Chassis and one 8-slot I/O Bus chassis. CPU model ACPU12 adds a second 8-slot I/O Chassis and a second Power Chassis. Models ACPU13 and ACPU14 add a third and fourth I/O Chassis.

The Processor, Memory Bus Controller and GENIE I/O control boards use five card slots in the Processor Chassis. The three remaining card slots may each hold a memory board for up to 192 k memory in this chassis. The Memory Protect Option, if used, goes in card slot 3 (but will also work in slot 2) and then leaves room for a 128 k memory in the Processor Chassis.

By adding an 8-slot expansion chassis, additional memory boards may be placed in the CSU cabinet for a total 256 k MOS memory. Metal Oxide Semiconductor (MOS) memory boards come in two sizes, 32 k and 64 k (k = 1024). Only one 32 k memory board may be used and it must be the last section of memory.

The CSU options and their model numbers are:

- ACME11 Memory Expansion Chassis
- AXME32 32 k MOS Memory Board
- AXME64 64 k MOS Memory Board
- AXMP11 Memory Protect Board
- AFFP11 Firmware Floating Point
- ABBU11 MOS Memory Battery Backup

The Firmware Floating Point Option is a set of PROMs (Programmable Read Only Memory) which plug into the Processor Control Board. With this option, floating point instructions are executed about ten times faster than with a standard quasi software package.

The optional Memory Battery Backup package prevents loss of MOS memory contents during power outages of 15 minutes or less. If memory contents are lost, the standard Auto Reboot or Manual Program Load function will reload the main MOS memory from bulk storage.

The CSU cabinet may have up to four 8-slot GENIE Bus Chassis. Typically, each controller on the GENIE Bus uses one or two slots. When more I/O Bus space is needed, one or more Expansion Cabinets (see section 14) can be added next to the CSU cabinet. Refer to part 4.5 for a description of the GENIE I/O Bus Controller and GENIE Bus operation. See 4.5.1 for a description of the device controllers available for use on the GENIE I/O Bus.

4.1 PROGRAMMABLE ARITHMETIC UNIT

The Programmable Arithmetic Unit, sometimes called the "AU", may be thought of as a microprocessor with supporting registers, data paths and micro-control instructions. The AU controls the sequencing of the Central System Unit and of controllers external to the CSU. It performs calculations and logical operations, and it controls the distribution of data throughout the computer system. All of these functions are accomplished as the AU executes programs stored in main memory. It executes such programs by "fetching" coded instructions from the memory and executing them in sequence. The AU features a large machine instruction repertoire, designed especially for use in process control programs that run on a real-time basis, as conditions in the process change, and as operators direct the computer's control of the process.

4.1.1 Instructions

There are more than 100 variations of the six basic instruction types described below. New Byte, Field and Bus Control commands have been added to the standard 4000 series instruction set. Appendix C of this General Description explains each command.

- Full Operand instructions perform arithmetic operations, logical operations, Index Register control, data transfers to and from main memory, and program sequencing and branching.

- GEN 1 instructions manipulate data in the A Register, manipulate the J counter, and set or reset the Test Flip-Flop as the result of certain tests. The function to take place is specified by microcoding of the instruction word and a very large number of such instructions is possible. The defined GEN 1 instructions are described in Appendix C.

- GEN 2 instructions are used mostly with GENIE I/O device controllers. They are used to input or output data and for test and control. The GEN 2 instructions perform some internal functions such as allowing or inhibiting APIs.

- GEN 3 instructions are used to shift the A and Q Registers either direction in a logical, circular, or arithmetic manner.

- Bus Control instructions are used to communicate with modules on the internal CPU/Memory Bus such as the Memory Protect or Memory Bus Controller units.

- Quasi instructions link the running program to a subroutine. A Quasi operation code causes the next instruction to be fetched from a dedicated memory address. This memory address is usually (but not always) equivalent to the Quasi operation code (bits 18-23). Quasi instructions store their effective operand in memory location 2 where the subroutine can find and use it to perform the desired function. The subroutine is provided by standard RTMOS software and could contain one or many other instructions.

4.1.2 Principal Registers, Counters, and Indicators

The principal functional components of the Arithmetic Unit are described in the following paragraphs. Fig. 4-1 indicates the major information paths between these components.

- Accumulator (A) Register. A 24-bit (23 bits plus sign) register which stores data for arithmetic operations, bit manipulation, logical operations, and temporary storage for data being transferred in or out of the AU through the use of GEN 2 instructions. The A Register has left and right shifting capability, including double word shifting when the Q Register serves as an extension of the A Register.

- Q Register. Main memory location 10_8, also known as the Q Register assists the A Register in performing some instructions such as multiply or divide. The A and Q Registers are coupled together as a 48-bit register for double length shift commands such as DLA, DRC, DLL, etc.

- Memory Data (MD) Register. A 24-bit register which normally contains the last word read from memory.

- Memory Address (MA) Register. An 18-bit register which tells the memory where to store or fetch an item. GEN type commands use it to control shifting of certain registers.

- Program Counter (P) Register. Bits 0-17 of this register hold the memory address of the next instruction. The P count is usually advanced by 1 while executing a program but not always. GEN 2 jump instructions can increment the P count by two when testing for ready or error conditions. Branch instructions load the P counter with a new address, from which program sequencing will continue. Only the lower 14-bits of an instruction may be used to specify a memory address but the P count can be extended by relative addressing or indexing.

  P Register bits 23-18 are used for status indicators as follows:

  18 IAI2, Inhibit all interrupts

  19 Memory Protect enabled

  20 Test Flip-Flop indicator

  21 PAI Flip-Flop (Permit level two API's.)

  22 Overflow Flip-Flop

  23 Floating Point Mode indicator

- Index Registers. Main memory locations one through seven are used as indexing registers. Index registers are easily incremented or decremented. When an instruction calls for indexing, the lower 18 bits from an Index register are added to the instruction operand. Indexing is useful for memory address modification or when setting up or reading from a table.

- J Counter. A 5-bit counter chiefly used with GEN 1 commands to keep a tally of bit-counting operations. It is read with the LXC instruction.

- Overflow Flip-Flop. The Overflow Flip-Flop is set when arithmetic overflow occurs. Overflow occurs when the result of an arithmetic operation is a number whose magnitude is greater than can be stored in a 23-bit register for single word results, or a 46-bit register for double word results. The status of this flip-flop is indicated by P Register, bit 22.

- Test Flip-Flop. The Test Flip-Flop is set or cleared when a test condition, which must be retained for subsequent action, occurs. The test conditions are defined by full operand instructions DMT and TXH, and by numerous Test Flip-Flop related GEN 1 commands. The status of the flip-flop is indicated by P Register, bit 20.

> **NOTE**
>
> Contents of the following registers cannot be displayed on the Programming and Maintenance console.

- X, K, and CI Registers. These are all internal registers. The 3-bit Index (X) Register is loaded with bits 17-15 of an indexed instruction. The K Register usually contains the last constant emitted by a microcoded instruction and the 48-bit CI Register acts like an instruction register for the microcoded control instructions.

- I Register. An internal register which holds an instruction which it is decoded and executed.

- B Register. A 24-bit internal register used to store addresses and temporary data results. It helps to execute some of the GEN 1 and 3 commands, also multiply and divide commands.

- ALU and Microprocessor. The Arithmetic Logic Unit element has two inputs: A and B. The registers shown on Fig. 4-1 are selectively connected as source inputs A or B. Control instructions (firmware) tell the ALU element to perform one of 32 functions. Typical functions would be: add A and B, complement A, output just A or just B, output 1's or 0's. The firmware also selects a destination for the ALU output. The ALU, stored control instructions and associated registers make up a "microprocessor" which executes "macro-instructions" from main memory.

4.1.3 Main Memory Addressing

4.1.3.1 Summary of Addressing Techniques

A Full Operand instruction has a 14-bit operand field (bits 13 through 0) and can, therefore, directly address any of up to 16,384 main memory locations. When relative addressing is used, a single instruction can address any location within +8191 to -8192 locations from the one containing the instruction. Using indexing, an instruction can address up to 256 k (k = 1024) of memory.

The memory addressing capability of the Arithmetic Unit contributes to the system's speed and facilitates programming. The relative addressing hardware allows the Real-Time Multiprogramming Operating System (RTMOS) to make optimum use of main memory by finding room for programs to be run and dynamically relocating the programs as required with no changes in operand coding. Addressing outside the program area is normally necessary only for communication with the resident portion of RTMOS, which is in lower memory and can be addressed directly. System throughput is maximized in that paging and indirect addressing are usually not necessary, and indexing is used only infrequently for large address modifications, or when it is advantageous, such as in modifying an operand by a constant or a variable value.

4.1.3.2 Detailed Description, Memory Addressing and Address Modification

In executing AU operations, instruction words and data are exchanged between the main memory and the AU. The locations in main memory from which, or to which, instruction words are to be transferred, are specified by a memory address word selected by the Memory Address Register for application to the Memory/CPU Bus address lines. Memory addresses generated in the execution of instructions may be the direct address indicated by the instruction operand, or the address may be modified by the contents of an Index Register. The address may also be converted to an address relative to the instruction. Both Index and Relative Operand Modification may be specified in the same instruction word. Index Address Modification and Relative Address Modification function as described in the following:

- Index Address Modification. Main memory locations 1 through 7 are dedicated as Index Registers. When bits 15 through 17 of an instruction word are not equal to zero (except ABP, INX, TXH, LXK, LXC, LDX, STX, and DMT), index modification of the operand is specified. The modification consists of the addition of the contents of the 18 least significant

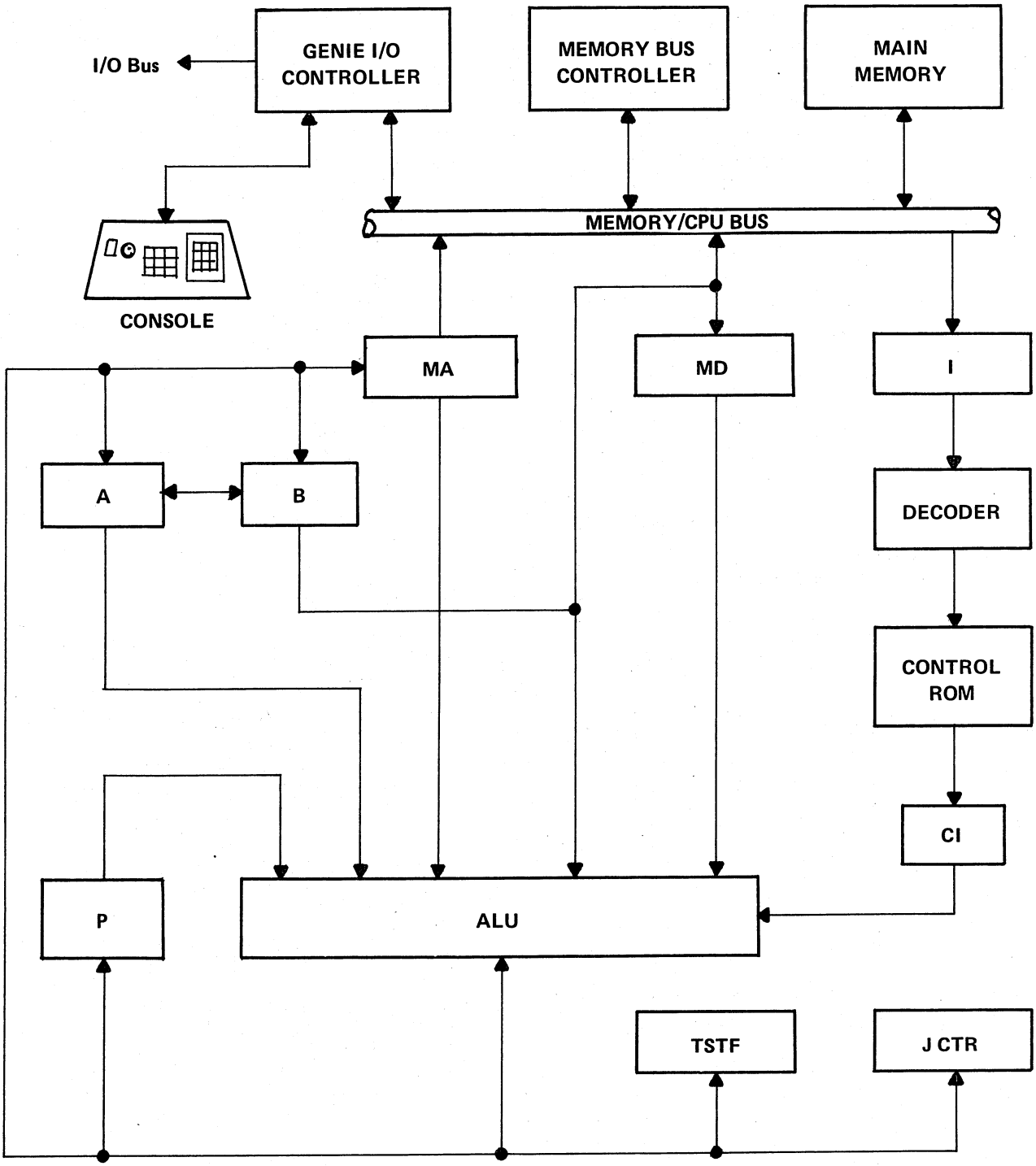


Fig. 4-1 Functional Block Diagram

bits of the Index Register specified by bits 15, 16, and 17 of the instruction word, to the operand of the instruction word.

- Relative Address Modification. When bit 14 of a Full Operand instruction word equals one, Relative Address Modification is specified. Relative addressing permits addressing of a location within plus 8,191 to minus 8,192 of the instruction address. If both bit 14 and bit 13 of the instruction word are set, the value of the Main Memory Address of the instruction word is subtracted from the operand field of the instruction word. If bit 14 of the instruction word is set and bit 13 is equal to zero, the value of the Main Memory Address is added to the operand. When 13 is set, indicating subtraction, the operand is in 2's complement form.

- Index Modification of GEN 1, 2, and 3 Instructions. The operand portion of the GEN 1, GEN 2, and GEN 3 instructions does not specify a memory address. Modification of the operand portion of such instructions by indexing may be accomplished but it changes the microcoding of the instruction, and therefore may produce an unexpected result. Index modification of GEN 2 instructions may be useful in modifying device addresses, and it is not uncommon to find such indexing used in hardware test and diagnostic programs, as it facilitates modifying such programs to run on systems with differing device addresses.

4.1.4 Arithmetic Operations

The AU performs both fixed point and floating point arithmetic operations. Fixed point arithmetic has the advantage of speed and somewhat greater precision than floating point. Floating point arithmetic has the advantage of ease of use by users and programmers and the ability to represent a much wider range of values. Fixed point operations require that the programmer/user keep track of the decimal point location and scaling used to represent the values, while floating point numbers can be converted by standard software routines to and from decimal values with a correctly positioned decimal point. See 4.1.5 for a description of the fixed and floating point data formats used in the 4500 system.

Fixed point arithmetic is accomplished by six Full Operand instructions: ADD (add), SUB (subtract), MPY (multiply), DVD (divide), DAD (double length add), and DSU (double length subtract). These instructions are described in Appendix C. These operations are fast and the 24-bit word length provides high precision with minimal need for the scaling of results. Less shifting of data and fewer instructions are required than might be necessary on 16-bit machines, thereby minimizing program size and running time.

In addition to the four single-word fixed point instructions, there are also double-word fixed point addition and subtraction instructions.

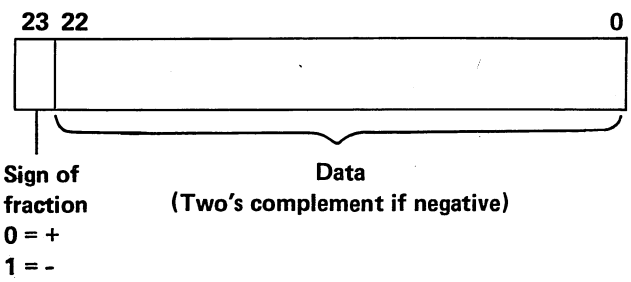
Floating point operations are accomplished by four Quasi instructions that are executed by standard Quasi subroutines if the Firmware Floating Point option (see 4.4) is not present, or by the execution of a single instruction if the Firmware Floating Point option is present. The four Quasi instructions are FAD (add), FSU (subtract), FMP (multiply), and FDV (divide). These instructions are defined in Appendix C. The hardware automatically uses the Firmware option when it is present.

Floating point operations will be single or double precision, depending on the state of the Floating Point Mode indicator. The Floating Point Mode is determined by the Floating Mode Shift (FMS) instruction.

4.1.5 Arithmetic Data Formats

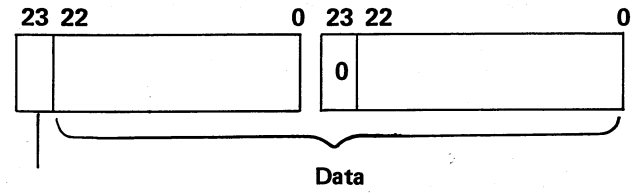
As indicated in the preceding discussion of the arithmetic operations, fixed point arithmetic operations result in either a single-word format or a double-word format. The fixed point formats represent negative numbers in two's complement form. Where the double-word format is in use, the sign bit of the most significant word is the sign of the entire number, and the sign bit of the second word is ignored. This is illustrated in the following sketches.

Single-word fixed point:



Range; +8,388,607 to -8,388,608

Double-word fixed point:

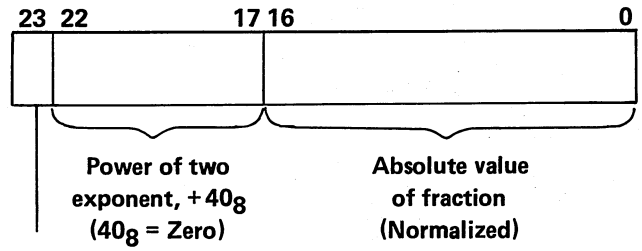


Sign of fraction
0 = +
1 = -

Range; +70,368,744,177,663 to -70,368,744,177,664

Floating point arithmetic operations may be in single-word or double-word formats as indicated in the following sketches.

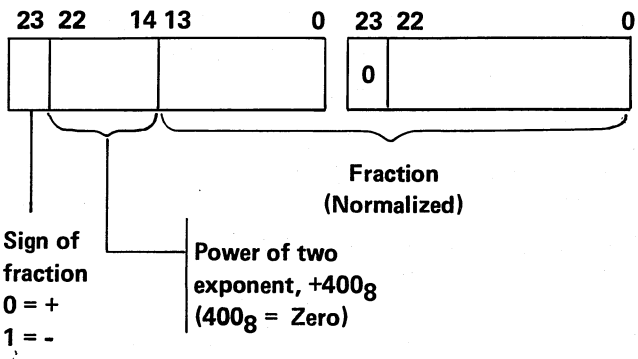
Single-word floating point:



Sign of fraction
0 = +
1 = -

Range (approximate); $\pm 2.15 \times 10^{\pm 9}$

Double-word floating point:



Sign of fraction
0 = +
1 = -

Range (approximate); $\pm 5.8 \times 10^{\pm 76}$

The Firmware Floating Point option (see 4.4) performs single-word floating point operations as much as 20 times faster than the Quasi routines.

4.1.6 Logical, Bit Manipulation, Field, Byte and Shifting Operations

Process conditions are stored efficiently in the TDC 4500 system because logical variables which originate from process contacts, logic voltage inputs, and process operator consoles can be stored as individual bits in the 24-bit computer data words. An extensive set of hardware-implemented logical instructions provides the means by which the computer evaluates and acts upon these logical variables. These powerful instructions provide a means for efficient manipulation of logical process data without extensive and complex masking operations used by our competitors. The following instructions are described in detail in Appendix C.

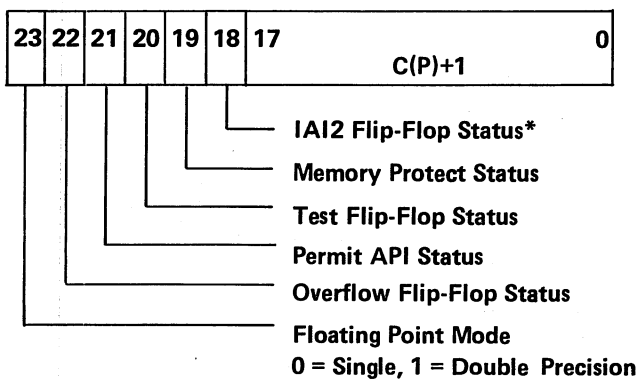
- Word length logical operations are accomplished by Full Operand instructions ANA, ERA, and ORA.
- Individual bit manipulations and bit tests are provided by GEN 1 instructions CBK, IBK, LDO, RBK, ROD, SBK, SEV, SOD, TER, TES, TEV, TOD, TOR, and TOS.
- Bit counting is provided by GEN 1 instructions CLO, CLZ, CMO, and CMZ.
- Bit manipulations and register tests are accomplished by GEN 1 instructions CPL, LBM, LDZ, LMO, NEG, REV, RNZ, SNZ, TNM, TNZ, TSC, TZC, and TZE.
- Operations which copy part of a specified memory location into the A Register are provided by the Byte and Field commands LBY, LBI, SBI, LDF, and STF.
- Comparison operations are performed by TXH, CME, CML, and some of the GEN 1 register test operations.
- Single-word data shifts are accomplished by GEN 1 instructions SRA, SRC, and SRL, and by GEN 3 instructions SLA, SLL, and SLC. These include arithmetic, logical, and circular shifts.
- Double-word data shifts are provided by GEN 3 instructions DLA, DLL, DRA, DRC, and DRL. These include arithmetic, logical and circular shifts between the A and Q Registers (see 4.1.2).

4.1.7 Subroutine Linkage

Main memory utilization is improved and running programs can be made more efficient if maximum utilization is made of subroutines. A subroutine is a program module that performs a function used repeatedly by one or more programs.

If the computer hardware provides a means of saving the status of the principal control flip-flops and the current program count before branching to a subroutine, and is able to restore this information in the hardware when the execution of the subroutine is completed, then the subroutine may be included at any point in any program, and may be executed almost as if it had been added to the instruction repertoire. This type of subroutine linkage is provided in the 4500 system by Full Operand instructions SPB (Save Place and Branch), and LPR (Load Place and Restore).

SPB stores the required information in memory location one in the form shown by the following sketch, and it inhibits inhibitable interrupts. If the subroutine uses memory location one, the first instruction in the subroutine should store the contents of location one in some other available location. LPR is the last instruction in the subroutine and it transfers the linkage information from its storage location to the appropriate flip-flops and the P Register. LPR causes the main program to resume at the location following the SPB if the subroutine left the stored P count unaltered, or it may return at a point determined by the subroutine, which is indicative of its outcome. Refer to Appendix C for additional details pertaining to the SPB and LPR instructions.



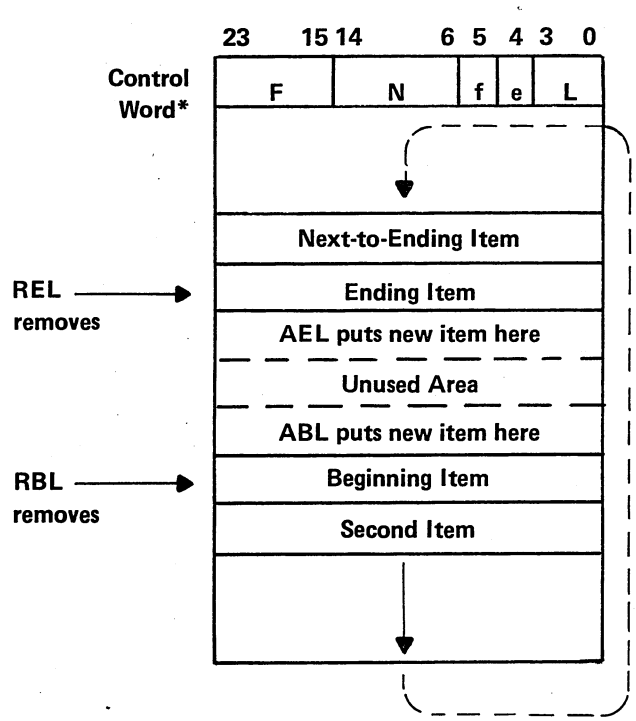
*Saved by SPB, but not restored by LPR.

Subroutine Linkage Information Word

4.1.8 Circular Lists

Circular lists are used to store data for input and output operations and for inter-program communication. They are configured and maintained by a subset of List instructions. A program that wishes to use the list needs to know only the address of a control word at the beginning of the list. Programs appending data to, and removing data from the lists can operate at different times and different speeds.

List instructions ABL and AEL append data to the beginning and end of the list, respectively. RBL and REL remove data from the beginning and end of the list. The list appears in memory as indicated in the following sketch.



*F = location of next beginning item
N = number of items in list
f,e = list is (e) empty, list is (f) full
L = length of list

Circular List

4.1.9 TIM/TOM Feature

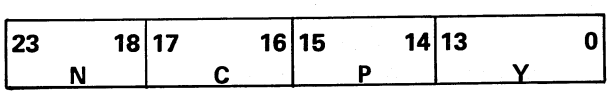
While data may be transferred between the A Register and the input/output modules and peripheral devices by means of GEN 2 instructions, the TIM/TOM hardware provides interrupt driven tabular data exchanges that are faster and require less programming effort. The Table Input to Memory/Table Output from Memory hardware provides a path through the AU to or from main memory for the transfer of characters 6, 8, 12, or 24 bits in length, without disturbing the programmable registers or flip-flops in the AU. Each such data exchange is initiated by an interrupt from an activated I/O controller on the GENIE I/O Bus (see 4.5).

The TIM/TOM feature makes effective use of the interrupt structure in the 4500 Central Processor to provide high throughput with minimal disturbance to the running program. When data is transferred through a high speed I/O channel, such as through the GENIE I/O Bus, the running program is delayed slightly. Then, the running program resumes where it was interrupted on completion of a TIM/TOM transfer, without the necessity of saving or restoring of information related to the program.

Each TIM/TOM channel provides for communication in one direction (input or output) and each channel is associated with a data exchange API and an echo/end-of-record API (see 4.3.2). An input/output device, such as an I/O typer requires two TIM/TOM channels. Theoretically, a system can have as many TIM/TOM channels as the number of possible GENIE I/O Bus controller device addresses or 256 channels. Since any practical system would have several GENIE Bus device addresses and corresponding API response addresses assigned to other functions, the maximum number of TIM/TOM channels is less than 256.

The TIM/TOM hardware makes efficient use of main memory because it can pack or unpack 1, 2, 3, or 4 characters per 24-bit word, as required by the I/O device or module. The sequence of events in a TIM/TOM operation is as follows:

1. The program loads the main memory location serving as the API response address with an appropriate TIM/TOM control word.



N = One's complement of number (up to 63_{10}) of words to be transferred.

C = Number of characters remaining to be packed into or unpacked from a word (normally set initially equal to P).

P = The number of characters (1, 2, 3, or 4) to be packed into or unpacked from each word:

00 = 4 characters

01 = 3 characters

10 = 2 characters

11 = 1 character

Y = One less than the memory address of the data table.

2. After the I/O controller has been activated and when it has a character ready for transfer or is ready to accept an output character, a data exchange API is generated. I/O controllers are typically activated by a GEN 2 OPR instruction, and remain activated until all characters in a table or record are transferred.

3. When an interruptible instruction in the program sequence is encountered, the running program is temporarily suspended, the control word is transferred from memory to the AU, the control word is updated, the character is transferred, and the control word is returned to memory.

4. Steps 2 and 3 are repeated each time an API occurs, until the proper number of words has been transferred, at which time the AU returns an "echo" to the I/O controller, which causes an echo API to be generated.

5. The echo API response location typically contains an SPB instruction (see 4.1.7) which causes the program to execute a subroutine that either repeats step 1, if appropriate, or it may deactivate the I/O controller because the operation is complete. The I/O controller may initiate the same API when it detects an end-of-record character in the data stream. The subroutine thus initiated may repeat step 1 if another record is to be transferred, or it may discontinue the operation. Typically, a GEN 2 JCB instruction will determine that the controller is not busy, if an end-of-record character was detected. A GEN 2 ABT instruction issued to a controller also typically causes an end-of-record API to be generated and sets the controller "not busy".

The transfer sequence is, of course, dependent upon the API's associated with the I/O controller not being inhibited or masked. The AU logic guarantees that at least one program instruction will be executed between each TIM/TOM transfer.

4.1.10 Timekeeping

Real-time and elapsed-time clock information for the operating system is normally derived from the Line Frequency Timer, a component of the I/O Controller. This timer derives logic level timing pulses from the input power line frequency. The pulses generated by the Line Frequency Timer may be pin selected to occur at the 60 Hz line frequency (50 Hz on systems using 50 Hz power) or at twice the line frequency (120 or 100 Hz). They are used to generate a system clock API (location 202) and clock echo API (location 203).

System timekeeping is accomplished by the Real-Time Multiprogramming Operating System (RTMOS) through the use of a Full Operand Decrement Memory and Test (DMT) instruction stored in the API response address for the system clock API. DMT acts as a one instruction subroutine by decrementing a count preset by the program in a designated main memory location. When the count passes from zero to minus one, the DMT instruction generates the system clock echo, which informs RTMOS that the predetermined time interval has passed. RTMOS then takes appropriate action and reloads the count location. Each line frequency cycle counted interrupts the running program for only 2.2 microseconds, and none of the AU contents are disturbed. Refer to 4.3 for a more detailed description of API operation.

Timer Alarm Package option ATAP11 contains a 2 kHz (± .01%) programmable clock for precision timing. Interrupts result from clock generator output and DMT echo. The complete Timer Alarm Package is described in 4.7.

4.1.11 Stall Alarm

This Arithmetic Unit feature is used to detect a program or hardware malfunction which causes a delay in program sequencing. One of three stall-time intervals may be selected by a jumper clip. The intervals are 64, 128, or 256 line frequency clock cycles, which equals 1.07, 2.13, or 4.27 seconds at 60 Hz.

The first Set Stall Alarm (SSA) instruction activates the stall timer. Other SSA instructions are placed at appropriate points in the running program (normally in RTMOS), and when executed, SSA restarts the timer. If a delay occurs which allows the timer to "time out", a Stall Alarm signal is generated. This signal illuminates the Alarm indicator on the Programming and Mainentance Console (see 4.1.14) and it is available as one of the system alarms for external use (see 4.7). A Jumper Clip option will let the Stall Alarm generate a "Reset" signal to initialize or restart the system.

The alarm indication may be cleared by the execution of SSA, by operating the Stall Lockout switch on the Programming and Maintenance Console while the console is enabled through its key switch, or by initializing the system hardware.

4.1.12 Memory Protect Option

The AXMP11 Memory Protect option provides efficient and comprehensive protection of process-related programs while new programs are being designed and debugged on line under the FREETIME IV program system. Memory protection is a hardware/software scheme that provides read-write-branch protection against illegal program operations, as well as protection from illegal I/O operations by programs running in the protected mode. The Memory Protect Controller board is normally installed in card slot three (but will work in slot two) of the Processor Chassis.

When memory protection is used, main memory is divided into 128 word blocks, each of which is assigned one of the four protection classes, shown in Fig. 4-2.

As normally used, Memory Protect is set up through the FREETIME IV Test program which assigns the protection codes needed to prevent interference to other programs. The classes are assigned by storing a protection code for each memory block in the Memory Protect Controller board. This is done by an LPM command with the A and Q Registers as shown in Fig. 4-2.

Memory Protect rules and functions:

1. Memory Protect is activated by execution of the LPR instruction with bit 19 of the operand equal to one (and provided that an Enable/Disable switch on the Memory Protect Controller is in the "ON" position). Bit 19 in subsequent LPR commands will be ignored until Memory Protect is deactivated.

2. Memory Protect is deactivated by the execution of any trap, the execution of an SPB in an API response address, or when the Enable/Disable switch on the Memory Protect Controller board is placed in the "OFF" position.

3. When Memory Protect is active, external GEN 2 and JND instructions may not be executed. Attempted execution of a GEN 2 results in an illegal instruction trap. This prevents interference with the I/O channels and devices by programs running in the protected mode.

4. Violation of the protection class for any protected main memory block results in a Memory Protect Trap.

5. When a trap occurs, the instruction stored at the trap address is fetched and executed. As used by FREETIME IV, this will be an SPB instruction which deactivates Memory Protect and branches the program to a corrective routine. The trap locations are:

   20_8 Normal M/P Violation

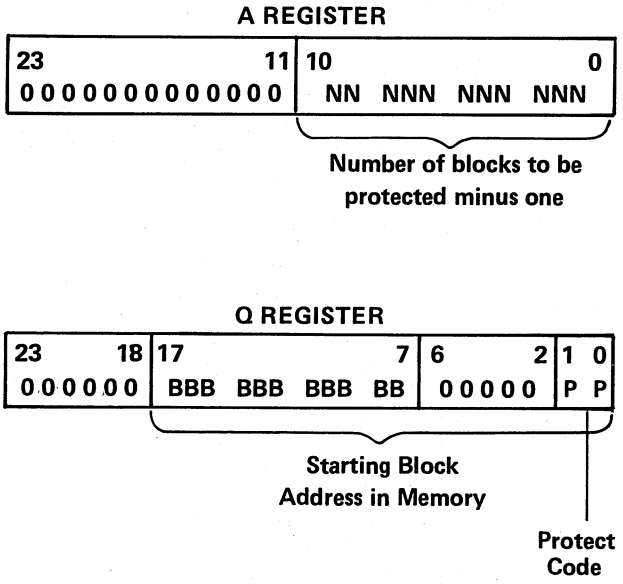
   31_8 Object of an SPB

6. If a trap occurs, the address of the instruction causing the trap is stored in location 21_8 - bits 0-17, and if it is a trap 20, bits 19 and 18 have the following meaning:

19	18	Meaning
0	0	Violation on data fetch
0	1	Violation on data store
1	0	Violation on instruction fetch

   If it is a trap 31, the address generated by the SPB is stored in location 27_8 - bits 0-17.

7. When Memory Protect is active, execution time of store type instructions is increased by approximately 10%. SPB instructions are extended by .45 microseconds and read/fetch operations are not affected. Memory Protect is normally activated through the FREETIME IV Test mode when testing a new program. When a Memory Protect Trap occurs, the FREETIME IV software prints diagnostic information on a system typer which indicates the location and nature of the program error that caused the violation. FREETIME IV allows the programmer to specify the degree of constraints for the program he is debugging, and to remove constraints gradually as he identifies and corrects errors, progressing toward his goal of an error free program. I/O operations are permitted, if specified as allowable by the programmer, by temporarily deactivating Memory Protect.



The four classes of protections are:

Protect Code	
11	The program may read, store, or branch anywhere in the block.
01	The program may read or branch in the block but may not store.
10	The program may read or write in the block but may not fetch instructions.
00	No access is permitted within the block.

NOTE: When Memory Protect is enabled, locations $0\text{-}10_8$ (the Index and Q Registers) are in a status equivalent to protect code "10".

Fig. 4-2 A and Q Register Format With LPM Command

4.1.13 Interrupt Watchdog

This feature provides assurance that programming errors will not excessively delay the servicing of Automatic Program Interrupts (API's). The Watchdog checks that API's inhibited by GEN 2 instructions IAI1 and IAI2 are serviced within predetermined time limits. It does not check on the misuse of GEN 2 instruction AIM(Activate Interrupt Mask) issued to modules on the GENIE Bus (see 4.5). (For further definitions of these instructions refer to Appendix C and refer to 4.3 for information on API operation.)

The API Watchdog checks for these errors:

1. When use of the IAI2 instruction has inhibited all interrupts for an excessive period.

2. Failure to service interrupts because of a long string of non-interruptible instructions.

3. When the PAI flip-flop has been reset for an excessive period.

4. Failure to service any interrupt request which has been present for an excessive period.

Checks 1 and 2 are made by counting memory cycles on the Memory/CPU Bus. If the IAI2 condition is still true, or if no interrupt has been serviced after 512 or 2048 CPU memory cycles (pin selectable), the Watchdog Trap (memory location 24_8) is activated. The current contents of the P Register is stored in memory location 27_8. The next instruction to be executed is taken from trap location 24_8. The Interrupt Watchdog is then disabled until any interrupt is serviced.

Checks 3 and 4 are made by counting 16 cycles of power line frequency through the built-in Line Frequency Clock circuitry (267 ms at 60 Hz). If interrupts are continuously present for this time, monitor circuitry attempts to trigger the level 1 PAI Alarm Interrupt (location 201_8).

If power has been off, the Interrupt Watchdog monitors are not enabled until an interrupt has been serviced. They are then active whenever the Programming and Maintenance Console is disabled or when both Interrupts and Stall Alarms are permitted by their console lockout switches.

4.1.14 Programming and Maintenance Console

The Programming and Maintenance Console (Fig. 4-3) is a primary link between programmers and maintenance personnel and the interior of the Central Processor. It is mounted on the front door of the CSU in a position and attitude convenient to a person sitting or standing. The console is used to turn the system power on and off, to load and step through programs, and to display registers, indicators, and alarm status. It provides controls that enable or disable several principal system functions such as Automatic Program Interrupts and the Stall Alarm. The indicators are bright enough to be easily read from a perpendicular distance of six feet.

The Programming and Maintenance Console is not normally available to process operators. A key switch is provided which locks out the controls on the console which might disrupt the computer's operation if disturbed while on line.

When enabled, the console may be used to place the Central Processor in Halt mode. Data and instructions may then be

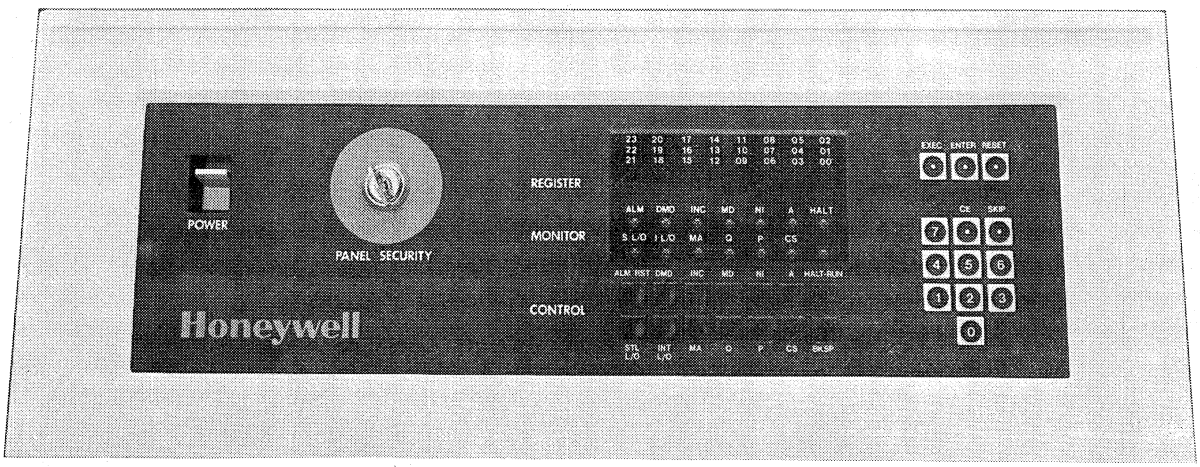


Fig. 4-3 Programming and Maintenance Console

entered in the A, P, NI, Q, MA, MD and CS Registers. In the Incremental mode, memory contents may be read sequentially. The program may be manually stepped through each instruction, and the content of the named registers observed, or it may be used to place the Central Processor in Run mode, where normal program sequencing takes place.

In either the Halt mode or the Run mode, the operator may enter data in the Console Switch (CS) Register for transfer to the A Register when GEN 2 instruction Read Console Switches (RCS) is executed, thus permitting the operator to communicate with the running program via the pattern in the console switches.

The Programming and Maintenance Console controls and indicators function as follows:

a. POWER On/Off - This switch turns on sequenced power to the CPU and generates an initialize signal. It works in all console modes (enabled or disabled). The Battery Backup Power Package option (if present) is wired directly to the power panel and is not affected by this switch. When this option is present memory power is supplied from the ac power lines even with the POWER switch off.

b. PANEL SECURITY - This two-position key switch either enables or disables the console. When enabled, either Halt or Run mode may be selected. All controls and displays may be used. When disabled, all registers may be displayed but only the CS register may be changed. The Console Switch Register and Demand button may be used to communicate with the program. When the console is disabled, the program is automatically set to Run mode with Interrupt Lock Out and Stall Lock Out features overridden. A remote console disable signal can be brought through the Optional Timer Alarm board to override the key switch and assure that the conosle is disabled (see 4.1.16).

c. REGISTER Displays - Eight octal displays show the contents of whichever register is selected, or information being entered through the keyboard. The selected register will be indicated on the MONITOR panel directly below the displays. Each octal digit represents three binary bits as shown just above each display. When displaying a register or memory and the console is enabled, the displays are updated approximately every quarter second. If the console is disabled, the displays are updated whenever a new display is selected.

d. MONITOR Indicators - Two rows of LED indicators just below the digital display panel tell which mode (Run/Halt) is selected, which register (A, P, Q, NI, CS, MA, or MD) is selected and show operating status (Demand flip-flop set, interrupts locked out, Stall Alarm locked out). The Alarm light may be turned on by:

Memory errors

Interrupt Watchdog

PAI Alarm

Programmed Alarm

GENIE Bus alarm line from any bus device

e. CONTROL Switches - Nineteen switches give the operator control over the CPU. With the console "disabled" (see Panel Security) an operator may set the Demand flip-flop, enter eight octal digits into the Console Switch Register and display any of the following:

A The Accumulator Register

P The Program Status and Location Counter register

Q The Q Register (memory location 10_8)

NI The Next Instruction Register holds the command which will normally be executed next. It is much like the 4000 series "B" Register

CS The Console Switch Register may be read by the running program with an RCS command. This register can be modified by the operator while the console is disabled.

When the console is enabled, the CPU may be in either the Run or Halt (single step) mode. In either mode, all of the previously described registers can be displayed and modified. The contents of memory locations may be displayed and changed using the Memory Address (MA) and Memory Data (MD) Registers*. Register information shown on the display is a "snapshot" of the register's contents (and not a direct constant monitor). AU firmware moves information between the console and actual hardware registers. In Run mode, most of the registers will be

*Except possibly when the area is memory protected.

changing rapidly as the program uses them, so a "snapshot" output to the console display is made about every quarter of a second (provided that the console is enabled and the cursor is not on).

An operator may enable/lock out the Stall Alarm or Interrupts using the alternate action pushbutton switches. The operator can also reset alarms (ALM RST), set the Demand flip-flop (DMD), RESET/Load the CPU (described later) or use the Incremental mode.

Incremental Mode causes the Memory Address register to be incremented after displaying or storing each memory location. This feature is very useful when storing a small hand loaded program or checking successive memory locations.

RESET/Program Load - This feature is always used with one of several keyboard switches. Pressing RESET does one of the following:

1. Initializes the CPU and sets the P Register to zero.

2. Moves a program load bootstrap routine from an internal ROM to upper main memory.

3. Coats memory with whatever pattern is in the CS Register.

Additional information is provided in part 4.1.15b, Using the Console. A "remote initialize" signal may also be brought in through the Optional Timer Alarm Package. (See 4.1.16.)

f. Keyboard Use - In addition to use with the RESET button as previously described, the keyboard is used with the following controls to select addresses and load registers:

ENTER - Tells the computer that you wish to load data into a selected register. When pressed, this button turns on the cursor causing the leftmost octal digit to blink. As each digit is entered through the keyboard, the cursor moves one position to the right. If more than eight digits are entered it will return to the most significant position.

CE - Clear Entry resets all eight display digits to 0's and puts the cursor in the leftmost digit position. Clear Entry is operable only when the cursor is on.

SKIP/BKSP - Skip moves the cursor right and Backspace moves it left. This feature is useful when you only want to change part of the display's contents.

EXEC - Execute has three uses:

1. If the cursor is on (blinking), EXEC steps data into the selected register and turns the cursor off.

2. If MA is selected or if MD and Incremental mode (INC) is selected, EXEC increments the Memory Address Register.

3. Otherwise EXEC causes the next instruction in a sequence to be executed.

4.1.15 Using the Console

a. Register Display or Entry - With the console enabled, any register may be selected for display. Memory Data (MD) will display the data contained at the address shown in the Memory Address (MA) Register. To change the contents of a register or the address in MA:

- Press ENTER - the cursor will blink at the leftmost position on the display.

- Enter new information through the keyboard using data keys 0-7, Clear Entry (CE), SKIP, and Backspace (BKSP) when helpful.

- Press Execute (EXEC) to load the display contents into the selected register or memory.

When using the MD display, sequential memory locations, Incremental mode (INC) may be set to advance the MA Register by one each time that EXEC is pressed. To use Incremental mode, press INC and then MD.

b. RESET and Program Load - The RESET button is pressed while holding a keyboard switch (0-7) down to initialize the CPU and cause one of the following results:

RESET and 0 - Sets P counter to address 0

RESET and 1 - Generates card reader bootstrap load routine (address 4002_8).

RESET and 2 - Generates paper tape bootstrap routine (address 4003_8).

RESET and 3 - Generates 1st bulk memory bootstrap load routine (address 4004_8).

RESET and 4 - Generates 2nd bulk memory bootstrap (address 4005_8).

RESET and 5 - Generates Floppy Disc bootstrap (address 4006_8).

RESET and 6 - Generates bulk bootstrap routine from address 4007_8.

RESET and 7 - Loads lower 64 k of main memory with the contents of the CS Register.

On 4500B processors, bootstrap routines try to load from the selected address first, but if that device fails to work properly, then loading is attempted from an alternate address. If the second device fails to work properly, then loading is again attempted from the first address. Proper operation is determined by testing the device controller's "ready" and "error" test lines. Loading attempts continue to alternate between the pair of addresses (unless one is a Floppy Disc) until either the load is completed successfully or the hardware is reset. Octal addresses 4004/4005 are a pair, and octal addresses 4006/4007 are a pair. Once started, a Floppy Disc automatically continues to execute the program load routine until it completes successfully or is reset.

Loading routines do not begin until the computer is set to Run mode. If necessary the operator may load the CS Register or change the bootstrap routine. Bootstrap routines will be placed in upper main memory and the P Register will hold the beginning memory address.

4.1.16 Timer Alarm Package

The optional ATAP11 Timer Alarm board normally plugs into the top slot of the first GENIE Bus chassis where special connections from the Processor Chassis are provided. This single electronic board contains:

- A precision 2 kHz (±.01%) programmable clock
- Eight programmable relays with output contacts
- Eight readable input lines
- Alarm and hardware status monitor circuits with individual relay output contacts
- A master alarm relay which is operated if any one of several selectable alarms or status conditions exist

These alarm and status conditions are monitored:

- Memory errors
- Stall alarm
- Stall alarm locked out*
- Console enabled
- Interrupts locked out*
- Programmable alarm status
- Two spares
- An external alarm input

There are also two remote control* input lines. One initializes the CSU from a distant point and the other overrides the key switch to disable the Programming and Maintenance Console.

Terminal strips behind the I/O chassis provide output connections from the relay contacts and connections to the readable input lines. The output contacts are rated for 10 Watts at .250 A or 100 Vdc maximum. The eight logic inputs expect either ground or an open condition.

Programming - The eight output relays are closed/opened by corresponding 1-0 bits in A Register positions 7-0 while executing a GEN 2 OUT command to the Timer Alarm board.

A GEN 2 IN command addressed to the Timer Alarm board will read in the status of the eight input lines to bit positions 7-0 of the A Register. Bits 7-4 may be shared (by Clip option) with one or more of the following functions:

Bit	Function
7	Remote Console Disable
6	Remote Initialize
5	Stall Alarm Locked Out
4	Interrupts Locked Out

The 2 kHz clock is turned on by a GEN2 OPR command with the S' bits (3, 4, 5) equal to 001. Unless masked, the clock then generates an interrupt for each clock cycle. A DMT echo is also provided. The clock is turned off by an OPR command with S' bits equal to 0's, or an ABT. The interrupt address is determined by the address set into the Timer Alarm board's switchpack (see 4.3.1).

Additional ATAP11 boards are sometimes used to provide extra clock timers or extra digital I/O points. In such cases the board may be used in any available card slot but computer alarm and remote control functions can only be used when the board is in the top slot of the first I/O chassis.

*These four signals (if selected) each take up one of the eight input lines.

4.1.17 Traps

Traps are triggered by serious or important conditions within the processor. When a trap occurs, the P Register and its indicators are usually saved in memory location 27_8 and related information is stored in location 21_8. The Trapping Mode, Test, PAI, Overflow, and Floating Point Mode indicators are reset. Finally, the contents of the trap location are executed. The TDC 4500 traps are:

Location	Cause
20_8	Memory Protect Violation
22_8	Power Fail Restart
23_8	Illegal Instruction
24_8	Interrupt Watchdog
25_8	Memory Error (on CPU Transaction)
26_8	GENIE Bus Arbitration Error
30_8	Memory Error (on Interrupt Service)
31_8	SPB Memory Protect Violation

The information saved in locations 21_8 and 27_8 is:

Trap	Location 21_8	Location 27_8
20	Address of last valid instruction, also status information - see 4.1.12	Not meaningful
22	Undefined	Undefined
23	Illegal Instruction	P Register
24	Not meaningful	P Register
25	Status - See 4.2	P Register
26	Not meaningful	P Register
30	Status - see 4.2	P Register
31	Address of SPB which caused trap - see 4.1.12	Address generated by SPB

Most traps are discussed in the section where they apply; the remaining ones are described here.

a. Illegal Instruction. An illegal instruction is any of the following when Memory Protect is shut off:

Any GEN 1 instruction with bits 11, 12, and 13 set.

Any GEN 1 with bit 8 reset and bits 5 or 6 set and bits 9 or 10 set.

Any GEN 2 with bits 14-0 in the range 00000 through 03777 except IAI2 and LPM.

Any GEN 2 with bits 11-0 (GENIE Bus address) in the range 1000_8 through 3777_8 (4500B only).

A Byte instruction referencing a Byte pointer with bits 22 and 23 set.

Any instruction with op-code 74 and bits 12 and 13 set.

When Memory Protect is enabled, the following instructions will cause an Illegal instruction trap:

Any instruction which is illegal with Memory Protect off.

Any external GEN 2.

JND or LPM

Any Control Bus instruction (op-code 27_8)

The Illegal instruction is stored in memory location 21_8 and the Trap instruction in location 23_8 is executed.

b. GENIE Bus Arbitration Error. If the GENIE I/O controller tries to service an interrupt but gets no response or detects a parity error while trying to determine the Interrupt address, then it triggers trap 26. The information stored in location 21_8 is not meaningful.

4.2 MOS MEMORY

Metal Oxide Semiconductor (MOS) memory is the working memory for the TDC 4500 Central Processor, where data and instructions currently in use by the running program are stored. This memory has a 600 ns cycle time and internally generates a refresh pulse every 2 ms to hold its contents. Each cell from location 11_8 and beyond is 30 bits wide. 24 bits are stored data and the other six bits are used for Error Detection And Correction (EDAC) by the Memory Bus Controller. Memory locations $0\text{-}10_8$ are high speed 24-bit registers contained on the Memory Bus Controller board.

Memory boards are available in the following sizes: (k = 1024 words)

32 k Model AXME32

64 k Model AXME64

Each memory board contains a set of switches to hold its beginning address. Address switches on each 32 k or 64 k board are in terms of 64 k, therefore if a 32 k memory board is put in a system, it must be used as the final part of memory to provide continuous addresses. One 32 k memory board may be used with up to three 64 k boards.

Using an optional Memory Expansion chassis, the 4500's present maximum capacity is 256 k.

4.2.1 Error Detection and Correction

The Memory Bus Controller (MBC) monitors access to the MOS Memory. If an error is detected, one of the following memory errors may result:

Yellow Error - A single bit of memory data was read incorrectly but has been automatically corrected. This condition may be detected and reset by CBR/CBW commands. The MBC detects and corrects all single bit memory errors.

Red Error - If more than one bit is incorrect in a word read from memory the red error results. If the MBC should detect one of these multiple bit errors it triggers one of the following traps:

Location 25_8 Memory error on CPU transaction

Location 30_8 Memory error on TIM/TOM or interrupt service

A trap of this type stores the Memory Bus Controller status into location 21_8. The P Register contents are stored in location 27_8 and the instruction in the trap location is executed.

Blue Error - This error may be caused by an illegal memory address or by failure of the memory to respond due to component failure. The same traps described above will result.

A software trap routine can distinguish between the error types by testing the contents of location 21_8 after trapping. Bits 0, 1, or 2 will be set if a yellow, red, or blue error (respectively) has occurred. Bit 3 will be set if the Stop On Error flip-flop is set.

The Stop On Error flip-flop may be set or cleared with a CBW command (set by A Register bit 8 = 1, reset by bit 7 = 1). When it is set, a red or blue error will lock out any further access to memory. When the flip-flop is reset, these errors will be trapped as already described. A switch on the MBC board may be placed in the "stop" position to guarantee that software cannot reset the Stop On Error flip-flop. One usage (when the switch is on) would be to command the flip-flop set knowing that in spite of mistaken sequencing, a nonrecoverable memory error will block further access to memory.

Normal operation will more likely leave the Stop On Error flip-flop fully under software control so that it can allow red or blue error trapping but set the Stop flip-flop to assure a full halt in case another of these errors occurs during the trap recovery routine. If another red or blue error occurs in the trap routine, the recovery method is to "reset" the system, either manually or by the Stall Alarm timeout.

4.3 AUTOMATIC PROGRAM INTERRUPTS

The Central Processor maintains continuous surveillance of important external and internal events through the Automatic Program Interrupt feature. While such events may originate in many different sources, all are processed through the GENIE I/O Bus, where the priorities are resolved by the I/O controllers and the Internal and External API Buffers on the bus.

No Central Processor time is consumed by such surveillance. When an interrupt is accepted, the running program is temporarily suspended, and one or more predetermined instructions are executed, to service the interrupt. After an interrupt has been serviced, control is returned to the running program with no loss of information or sequencing. This feature provides fast responses to process conditions, permits I/O devices to operate at their full rated speeds without special attention by the running programs, and through RTMOS, assures that programs are run in the appropriate order of priority, as time passes and conditions change.

The interrupting signals are referred to as Automatic Program Interrupts, "interrupts", or "API's". Each addressable controller on the GENIE I/O Bus can make one or two types of interrupt requests. These requests are referred to as "type 0" and "type 1". Type 0 requests have the higher priority of the two requests for one addressable controller and normally serve as data exchange, timekeeping, or event count API's. Type 1 requests have the next lower priority of the pair, and are normally used as end-of-record, transfer complete, or echo API's. Since there can theoretically be up to 256 addressable controllers on the GENIE I/O Bus, the maximum number of API's that can be monitored by the Central Processor is 512.

Interrupts from subsystems and devices not controlled from the GENIE I/O Bus are accepted by the API Buffers. Model

AIIE11 accepts up to eight logic level or contact closure interrupt signals from sources external to the computer system. Each of these buffers uses one of the available 256 GENIE I/O Bus addresses for each pair of interrupts.

4.3.1 Interrupt Addresses and Priorities

The relative priority of the interrupt requests from each controller on the GENIE I/O Bus is selected independently, and in any order, by jumper pins or switches on the modules (see 4.5 for a description of the bus structure). The priority of each interrupt request pair (type 0/type 1) on each controller is not related to the controller's device address, but the device address does indirectly indicate the interrupt response address in main memory to which program control is transferred when an interrupt is serviced. When the GENIE I/O Bus controller senses an interrupt request and determines that the request can be serviced, it applies an acknowledge signal to the bus, which causes the highest priority controller that is requesting an interrupt to return its device address to the GENIE I/O Bus controller. The GENIE I/O Bus controller then derives the API response per the following equation:

$$\text{Response Address} = 2(\text{DDD} - 300_8) + \text{Request Type}$$

Where DDD is the controller's device address, which can range from 400_8 to 777_8, and the request type is 0 or 1. Thus, the 512 response addresses in main memory range from 200_8 through 1177_8. (The DDD device address is actually contained in the K_3, K_2, and K_0 fields of the GEN 2 instruction words, and the K_1 field of such words may be used as an S' subfunction indicator. See 4.5 for additional GENIE Bus addressing considerations.)

The following GENIE I/O Bus controller addresses and their corresponding API response addresses are preassigned:

Interrupt Response Address	Function
200	Power Fail
201	PAI Timer
202	Line Frequency Timer
203	Line Frequency Timer Echo

4.3.2 Interrupt Types

Each I/O controller on the GENIE I/O Bus may make a type 0 interrupt request (data exchange, timekeeping, event counting) and/or a type 1 interrupt request (end-of-record, echo, transfer complete). The types of interrupts that result from the servicing of such requests, and the general functions of the instructions executed as they are serviced are as follows:

Timekeeping (clock) interrupts are generated by the Line Frequency Timer and the programmable 2 kHz clock in the optional Timer Alarm Package. Typically these periodic interrupts cause the execution of Full Operand instruction, DMT. This instruction acts as a one instruction subroutine which decrements a count preset by the program in the API response address. When the count passes from zero to minus one, the DMT instruction causes an "echo" API to be generated, which informs the timekeeping program that the time period has elapsed. The timekeeping API's which cause execution of DMT, are normally selected as non-inhibitable. The "echo" API's are normally selected as inhibitable.

Data Exchange API's are generated by input/output devices or communication channels to indicate that data is ready for transfer from the device or channel to the AU and memory or that the device or channel is ready to accept data. Such interrupts typically cause a TIM/TOM operation (4.1.9) and are normally selected as non-inhibitable.

End-of-Record and Transfer Complete interrupts are generated by input/output devices to indicate that the transfer of a complete block of data has been accomplished. Such interrupts typically cause the Full Operand instruction, SPB, to be executed, thereby retaining data pertinent to the interrupted program. while a routine is executed which prepares itself and the SCU for transfer of the next block of data, by storing new instructions or TIM/TOM control words in appropriate API response addresses, preparing new data tables, etc. Upon completion of the routine, return to the program is made through the use of the LDP or LPR instructions. This type of interrupt is normally inhibitable.

Echo interrupts are generated by the I/O controllers in response to an echo signal generated by the Arithmetic Unit when it determines that a DMT count has been fully decremented, a TIM table has become full, or a TOM table has been emptied. In some cases, I/O controllers request the same interrupt upon the receipt of an echo response from the AU, as upon the detection of an end-of-record condition by the controller. Echo interrupts are serviced by the execution of an SPB instruction in the response address location as described under "End-of-Record and Transfer Complete". Echo interrupts are normally inhibitable.

4.3.3 Inhibiting and Masking API's

While maximum system performance is generally attained by allowing API's to be serviced with minimal delays and as little restriction as possible, it is necessary to provide the running programs a means to inhibit groups of interrupts or individual type 0/type 1 interrupt pairs selectively. Certain instructions must also temporarily inhibit API servicing. Inhibited API's are not lost because the GENIE I/O Bus controllers retain all requests for API service until the requests are serviced. (Refer to 4.5.2 and to Appendix C for more detailed descriptions of the instructions mentioned here.)

When GEN 2 instruction IAI1 is executed, all inhibitable interrupts are inhibited until they are again permitted service by the execution of GEN 2 instruction PAI, or by Full Operand instruction LPR with bit 21 = 1 in the subroutine linkage information word (4.1.7).

If, while inhibitable API's are inhibited, GEN 2 instruction IAI2 is executed, all interrupts are inhibited until they are again permitted service by the execution of PAI or by LPR with bit 21 of the subroutine linkage information word set.

Each pair of interrupt requests from a GENIE I/O Bus controller may be masked by the execution of GEN 2 instruction AIM addressed to the controller. Each pair may be unmasked by the execution of GEN 2 instruction DIM addressed to the controller. AIM may be executed to mask the requests from a controller at any time, but it is good practice to mask requests while all interrupts are inhibited by IAI2, so that interrupts that are not masked will all be uninhibited at the same time..

All API's are inhibited when the API Enable/Disable switch on the Programming and Maintenance Console is in the Disable position.

The API Watchdog option (4.1.13) checks that API's are not inhibited for excessive periods of time by IAI1 and IAI2. It does not check on the misuse of AIM.

Since the program sequence might be altered or data may be lost if an API is serviced immediately after the execution of branch instructions, bit counting instructions, index register loading and testing instructions, and instructions that control the API subsystem, such instructions inhibit API's until one additional instruction is executed. Among these non-interruptible instructions are: BTS, BTR, LDP, LPR, LDX, SPB, OOM, TXH, XEC, CLO, CLZ, CMO, CMZ, AIM, IAI1, IAI2, PAI, DIM, and Quasi instructions.

API's can be "disabled" by storing a NOP (no operation) instruction in the response location if the normal instruction stored at that location is SPB or DMT. If the response location normally contains a TIM/TOM control word, the API can be disabled by storing a control word with the N field equal to 77_8. Disabled API's are lost as they are serviced.

4.4 FIRMWARE FLOATING POINT OPTION

The optional AFFP11 Firmware Floating Point option executes single or double precision Floating Point arithmetic operations faster than if the standard Quasi instruction subroutines are used for such operations. Refer to 4.1.4 for a discussion of the fixed point and floating point operations performed by the Arithmetic Unit and to 4.1.5 for a description of the fixed and floating point data formats. Floating point operations and data formats are the same when the Firmware option is used, as with the Quasi subroutine, except for the speed of operation and the replacement of the Quasi subroutine with a single instruction.

Here are typical execution times for the Firmware Floating Point instructions. These times are typical; they can be slightly shorter or longer. It depends on what numbers are used and sequencing delays:

Instruction	Single Precision	Double Precision
FAD	7.5 µs	25 µs
FSU	7.8 µs	25 µs
FMP	8.0 µs	19 µs
FDV	10.2 µs	34 µs
FLO	8.0 µs	18 µs
FIX	8.0 µs	55 µs approx.*

The Firmware Floating Point option may be installed at the factory or added to an existing TDC 4500 system at any time. A set of pre-programmed PROM's is inserted into sockets on one of the processor boards and a jumper clip is moved on the memory bus controller board. The same floating point operation codes are used for either the Quasi or Firmware routines.

*Double Precision FIX is executed as a standard Quasi.

4.5 GENIE I/O CONTROLLER AND BUS

The GENIE I/O Bus is the principal communications interface between the Central Processor and the system's process I/O controllers, peripheral devices, video displays, and remote communications channels. In theory, up to 256 separately addressable modules may be included on the bus, and bi-directional data transfers of up to 24 parallel bits may be made direct to main memory, through the AU via the TIM/TOM feature, or under direct control of the running program. Fig. 4-4 depicts the GENIE I/O Bus subsystem.

All three types of data transfers may be fully interleaved, with direct to memory transfers having priority over those through the Arithmetic Unit. API and direct to memory request priorities of the I/O controllers are selected on the individual modules, are not related to device addresses nor physical placement on the bus, and may be changed at any time. The maximum direct to memory transfer rate is every other memory cycle. The transfer rate through the AU is dependent on instruction execution times, the interruptibility of instructions in the running program and the mix of instructions. Maximum GENIE Bus throughput is one million words per second.

4.5.1 I/O Controller Complement

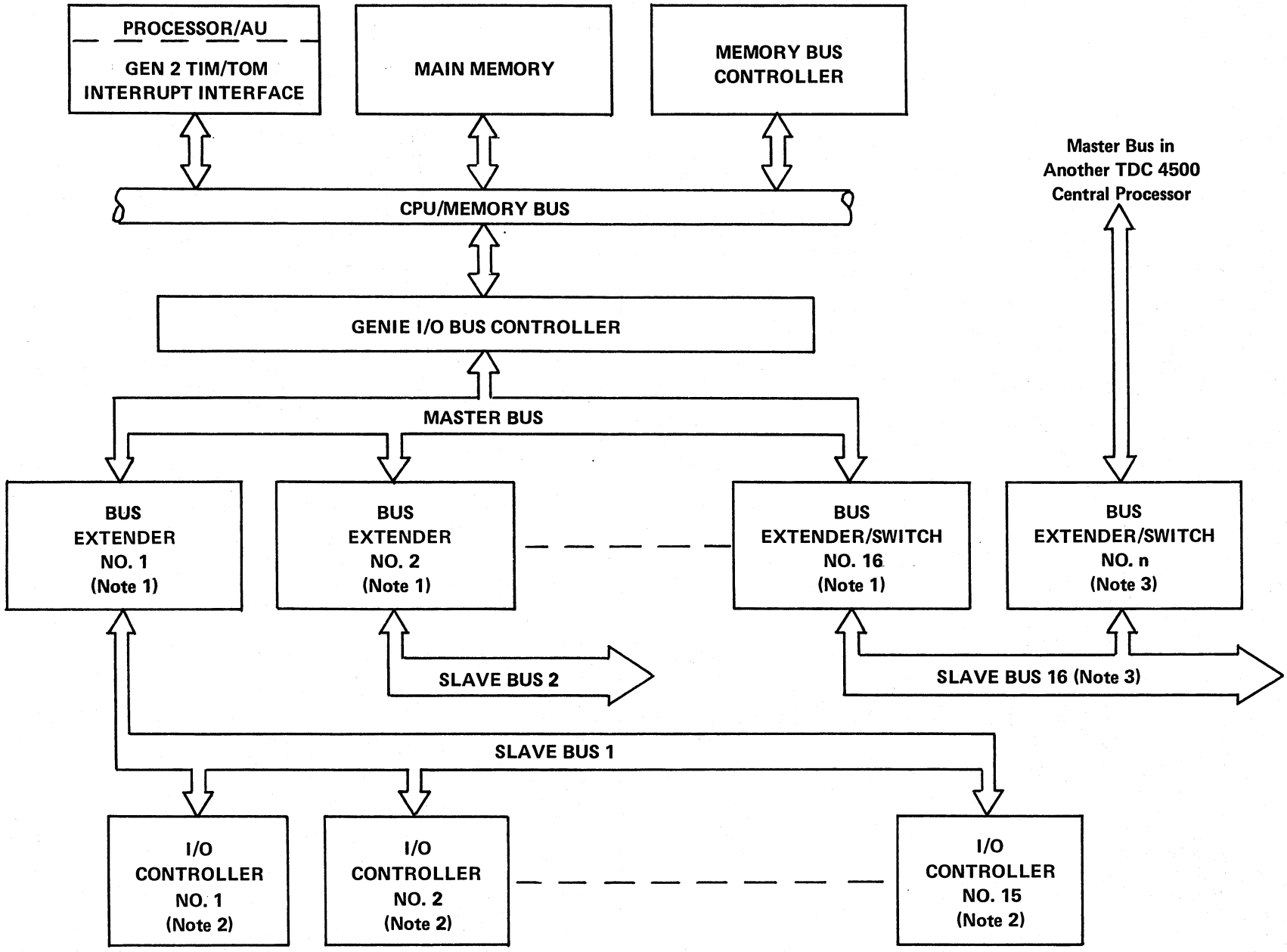
I/O controllers currently available for use on the GENIE I/O Bus, their major function, and the location of their description in the General Description are as follows. They may be implemented in any reasonable order and combination, up to the number of available GENIE I/O Bus device addresses, the number of available GENIE Bus Chassis slots, and the bus load drive capability available on the Master Bus and on Slave Buses (see Fig. 4-4).

- ADRM1 Drum Memory Unit Controller, drives one drum or Large Core Store Unit of up to 1.3 million word capacity, Sections 5, 18.
- ABMC1 Bulk Memory Controller, for use with disc, inter-system link or magnetic tape controllers.
- ADSC1 or ABMS12, 14 Moving Head Disc Controller, drives up to eight 16-million word Disc Units, Section 6.
- ABMS13, 14 Magnetic Tape Controller, drives up to four 800 or 1600 BPI transport units, Section 17.
- ABMS11 Inter-System Link, transfers up to 100,000 24-bit words/second between 4500 memories, Section 16.
- AIDH11 Data Hiway Interface to TDC 7100/2000 Process I/O equipment, Section 13.
- AXPV1 Honeywell Process Video HPV-1 Monochrome Video Interface, Section 10.
- APVB1 Honeywell Process Video HPV-2 Color Video Interface, Section 9.
- AXFD1 Floppy Disc Interface, Section 15.
- AXTC1 Telecontrol Interface to remote process, Section 13.
- AXPR1 Reader Drive, drives one Card Reader or one Paper Tape Reader, Section 8.
- AXPP1 Punch Drive, drives one Paper Tape Punch or one Card Punch, Section 8.
- AXLP1 Line Printer Drive, drives one Line Printer, Section 8.
- AXSP1 I/O Teleprinter Drive, drives TermiNet* Printer (300 or 1200) or Matrix Printer, Section 8.
- AXPV1 Asynchronous Communication Drive, interface for serial data link via data sets, Section 13.
- APDL1 Computer Interface Unit, 8 or 12-bit high speed parallel data link to another Central Processor, Section 13.
- AIIE1 Internal/External Interrupt module, accepts up to eight interrupts from non-GENIE Bus controllers in ASU or external, 4.3. Also accepts external (contact closure) interrupt signals.
- APID1 Digital Process Interface Controller, provides 2-port interface to Digital Process I/O Subsystem, Section 11.
- APIA1 Analog Input Controller, provides 2-port interface to Analog Input Subsystem, Section 12.
- ASDL1, 2, 3 Transparent Synchronous Data Link. Section 13.
- ATAP1 Timer Alarm Package, monitors alarms, has 2 kHz clock, eight digital I/O points (4.1.16).

The AIOC11 GENIE Bus Chassis accepts up to eight 15" controller boards. Typically, each controller occupies one or two board slots. The basic CSU cabinet can hold up to four 8-slot I/O chassis. I/O power supply ACPS11 is added to power the second, third, and fourth I/O chassis.

As Fig. 4-5 indicates, the master GENIE I/O Bus can accommodate up to 16 loads** which may be either AXBE11 Bus Extenders, AXES11 Extender/Switches or I/O controllers. Each extender type provides the drive capacity to accommodate 15 additional loads on the bus by creating a Slave Bus section. They may also be used as switches to permit a Slave Bus section to be shared by two, three, or four 4500 CSU's. The extenders occupy one slot in the GENIE Bus Chassis and are normally at the beginning of the Slave Bus section

*Registered Trademark of General Electric Co.
**Usually, each controller presents one load.



(For Notes, See Page 31)

Fig. 4-4 GENIE I/O Controller and Bus

they create. Where a Slave Bus is common to more than one CPU, extenders for each processor are installed next to each other. Only one CPU may switch its bus onto the Slave Bus at any time. AXBE11 Bus Extenders and AXES11 Extender Switches are identical except the AXES11 contains a "dead-man power supply". If chassis power fails at the slave bus, AXES11's stay "alive" by automatically taking power from their controlling CPU. In this way, they can still interrupt the CPU and return status information.

4.5.2 GENIE I/O Bus GEN 2 Instructions

The following GEN 2 instructions affect the GENIE I/O Bus controller and controllers on the bus. The functions of these instructions that are particularly related to the GENIE I/O Bus operation are described here. All GEN 2 instructions are described in Appendix C. GEN 2 instructions addressed to controllers on the bus are executed in approximately 2.5 microseconds (non-indexed).

The GEN 2 instruction words are encoded as follows:

23 21	20 18	17 15	14 12	11 9	8 6	5 3	2 0
2	5	X	S	D	D	S'	D

Where,

25 is the GEN 2 operation code.

X specifies the X Register, if any, to use for operand (DDS'D) modification.

S specifies the primary function to be performed. DDD are the GEN 2 K_3, K_2, and K_0 fields and define the I/O controller device address, which can range from 400_8 through 777_8.

S' specifies the subfunction, if any, to be performed.

25X0DDS'D = NOP, No Operation. NOP is ignored by the GENIE I/O subsystem.

25X1DD0D = ACT, Activate Interrupt. The function of ACT is not specifically defined for GENIE I/O Bus controllers, but it may be used for a special purpose. ACT would typically trigger an end-of-record interrupt request from the addressed device.

25X1DD6D = AIM, Activate Interrupt Mask. AIM masks the interrupt pair from device DDD. See 4.3.3.

25X1DD7D = DIM, Deactivate Interrupt Mask. DIM unmasks the interrupt pair from device DDD. See 4.3.3.

25X1DDS'D = ACT, AIM, DIM. Subfunctions may be defined in the future for S' = 1 through 5.

25X2DD0D = OPR, Operate. OPR initiates operation of controller DDD and any associated device, typically setting the controller "busy". Normally the first data exchange interrupt occurs after OPR is executed.

25X2DDS'D = OPR S'. OPR with S' equal to 1 through 7 may be used to specify the transfer of data from the A Register to the addressed controller for some special function, in addition to the normal functions of OPR.

NOTES for Fig. 4-4

1. **The Master Bus can accept up to 16 loads* consisting of Bus Extenders, Extender/Switches, or I/O Controllers. Any of the 16 loads not used for Extenders may be used for I/O Controllers. First interrupt priorities are selected on Extenders, then on I/O Controllers on Slave Bus. I/O Controllers on Master Bus select Master Bus (highest) interrupt priorities.**

2. **Each of up to 16 Slave Buses is created by an Extender. Each Slave Bus can accommodate up to 15 I/O Controller loads*. Interrupt priorities selected on I/O Controllers on Slave Bus are sub-priorities to the Extender priorities, so 256 interrupt pair priorities are available if there are 16 Slave Buses and 15 I/O Controller priorities on each Slave Bus, for a total of 512 interrupt priority levels.**

3. **A Slave Bus may be shared by two, three, or four TDC 4500 computer systems on a mutually exclusive basis, if the Master Bus in each of the sharing system is connected to a common Slave Bus through individual Bus Extender/Switches. The Bus Extender/Switches may be set up to select differing Master Bus interrupt priorities.**

*Usually, each PWB equals one load.

25X3DD0D = ABT, Abort. ABT terminates the operation of controller DDD and any associated device, typically setting the controller "not busy", and triggering an end-of-record interrupt. After the controller has gone "not busy", it is left in the same condition as if it had been initialized from the Programming and Maintenance Console or during a power-up sequence. ABT S' = 1 through 6 may be defined for specific subfunctions on the addressed controller.

25X34000 = ABT to GENIE Bus I/O Controller. This instruction initializes the GENIE Bus I/O Controller without affecting any of the controllers on the bus.

25X34070 = ABT to GENIE I/O Controller and all controllers on the Bus. This instruction initializes the GENIE I/O controller and all controllers on the GENIE I/O Bus.

25X4DD0D = OUT, Output to DDD. OUT transfers data from the A Register to the addressed controller. It is normally ignored if the addressed controller is not "busy". Where less than the full 24 bits of A Register data are transferred, the data transferred are in the least significant bits. OUT S' = 1 through 7 may be defined for specific subfunctions on the addressed controller.

25X5DD0D = IN, Input from DDD. IN transfers data from the addressed controller to the A Register. It is normally ignored if the addressed controller is not "busy". Where less than the full 24 bits of data are transferred, the data are transferred to the least significant A Register bits. IN S' = 1 through 7 may be defined for specific subfunctions on the addressed controller.

25X6DD0D = JNR, Jump if DDD Not Ready. JNR is used only to test the "ready/not ready" status of controllers having a single busy/ready test line. Controllers on the GENIE I/O Bus typically have both a busy test line and a data ready test line, and the latter is tested by JDR. If the addressed controller is in operation (not ready) program control is transferred to the second sequential location (P+2). If controller DDD is ready, program control continues at the next sequential location (P+1).

25X6DD2D = JCB, Jump if Channel Busy. JCB tests the "busy" line on the addressed controller. The controllers are typically set busy by the execution of OPR, but some input channels are set busy, at least temporarily, by an input demand, such as pushing the Interrupt button on a TermiNet printer or pushing the Break key on a teletypewriter. If controller DDD is busy, program control is transferred to the second sequential location (P+2). If it is not busy, program control continues at the next sequential location (P+1). Controllers typically request an end-of-record interrupt when they go from "busy" to "not busy".

25X6DD4D = JDR, Jump if Data Ready. JDR tests the "data ready" test line on the addressed controller. The data ready line is true when the controller is ready to transfer data to the AU via TIM or IN or when it is ready to accept data via TOM or OUT. The controllers typically request a data exchange API when data ready goes true. If data ready is true, program control is transferred to the second sequential location (P+2). If data ready is false, program control continues at the next sequential location (P+1).

25X7DD0D = JNE, Jump if No Error. JNE with S' = 0 tests the error line of the addressed controller. JNE with S'= 1 through 7 may define specific errors or classes of errors for specific controllers, any of which could be sensed, without being identified, by JNE S' = 0. If no error has been detected, program control is transferred to the second sequential location (P+2). If an error has been detected, program control is transferred to the next sequential location (P+1).

25X74000 = JNE, Jump if No GENIE Bus Deadman Timer Error. This instruction causes a jump (P+2) if the GENIE I/O Bus controller deadman timer has not timed out due to failure to receive a Slave Sync response from any controller in reply to a Grant or Master Sync signal from the GENIE I/O Bus controller. If the timer has timed out, program control is transferred to the next sequential location (P+1).

25030000 = IAI1, Inhibit Inhibitable Interrupts. IAI1 inhibits API requests that are selected on the GENIE Bus modules as inhibitable. See 4.3.3. IAI1 executed while in the state specified by IAI1 or IAI2 is ignored.

25000304 = IAI2, Inhibit All Interrupts. See 4.3.3. IAI2 executed while not in the state specified by IAI1 is ignored.

25020000 = PAI, Permit Automatic Program Interrupts. PAI permits the servicing of interrupts that are not masked. See 4.3.3.

4.5.3 Transfer Sequence - To and From AU

The sequences described here are those accomplished by the GENIE I/O Bus controller and controllers on the bus in responding to GEN 2 instructions addressed to controllers on the bus. The GEN 2 instructions can be divided into two classes. Those in the first class sense the busy, ready, error status of the addressed controller, and transfer data from the addressed controller to the Arithmetic Unit. Instructions in the second class transfer control information to the addressed controller and transfer data from the AU to the controller.

The IN instruction and the TIM function are in the first class. TIM appears to the GENIE I/O controller to be the same as the IN instruction. Data transferred by IN goes to the A Register, while data transferred by TIM goes to main memory via the AU. The OUT instruction and the TOM function are in the second class, and TOM appears to the GENIE I/O controller to be the same as the OUT instruction. Data transferred by OUT originates in the A Register, while data transferred by TOM originates in main memory and is transferred via the AU. OPR may also transfer control data or parameters from the A Register.

IN, TIM, JDR, JNR, JCB, JNE:

1. The GENIE I/O Bus Controller (IOC) goes busy and places the device address and action information (S and S') on the bus.

2. The IOC activates the Master Sync signal, which causes the controllers to examine the device address. The addressed controller self-selects.

3. The addressed controller places the requested status information or data on the bus and activates the Slave Sync signal.

4. The IOC picks up the data or status information and removes Master Sync.

5. The addressed controller removes Slave Sync and the data or status information.

6. The IOC goes ready for the next transaction.

OUT, TOM, AIM, DIM, OPR, ABT, and ACT:

1. The GENIE I/O Bus Controller (IOC) goes busy and places the device address, data (if any), and action information (S and S') on the bus.

2. The IOC activates the Master Sync signal, which causes the controllers on the bus to examine the device address. The addressed controller self-selects.

3. The addressed controller initiates the requested action and if data was presented, it accepts the data. It then activates the Slave Sync signal.

4. Upon sensing Slave Sync, the IOC removes the Master Sync signal, the address, action information, and data, and goes ready for the next transaction.

5. The addressed controller removes Slave Sync.

4.5.4 Transfer Sequence - Direct To and From Main Memory

Direct to Memory transfers (also referred to as "direct memory accesses" - DMA's) require little attention from the running program. A memory request from a controller on the GENIE Bus that occurs simultaneously with a request from the AU is serviced first. The Memory Bus Controller resolves priority when more than one user is requesting memory. It is possible for a user which has gained access to memory to temporarily lock out other requestors as is done by the AU while executing commands like DMT where an extra memory cycle is needed to complete the operation. DMA transfers can be to or from any memory address within 256 k (262,144 words).

Typically, prior to a DMA transfer, the program supplies the parameters of the transfer to the controller on the GENIE Bus that is to handle the transfer. These parameters typically include the starting address of the transfer area in main memory, the length of the transfer, and if appropriate, the starting address of the transfer area on the device attached to the controller. These parameters may be transferred by OPR or OUT instructions, and one of those instructions typically causes the controller on the bus to initiate the transfer sequence. When the transfer is complete, or if it is aborted for some reason, the controller typically requests a transfer complete interrupt (4.3.2).

DMA transfers consist of memory read and memory write transfers. The controller on the bus that is handling each transfer dictates whether it is a read or write, and whether it is a 24-bit word transfer, or an 8-bit byte transfer. If it is a byte transfer, the controller dictates which of the bytes in the memory word is to be transferred. All DMA transfers are asynchronous, and can occur at any time when the GENIE I/O Bus is not busy with some other transaction. The DMA request priority for each controller on the bus is the same as the API priority, and is selected by the same controls on the Bus Extender/Switches on the controllers.

Each word or byte transfer begins with the selection sequence:

1. A controller on the bus requiring access to memory activates the Memory Request signal on the bus.

2. If the GENIE I/O Bus Controller (IOC) is not busy or when it next goes not busy, it activates the Memory Acknowledge signal on the bus, which selects the highest priority controller on the bus that is requesting memory access.

3. The IOC activates Grant Sync, and in response, the selected controller places the address of the memory location to be accessed (up to 256 k of main memory) and the read, write, and word/byte information on the bus. The controller then activates the Slave Sync signal.

4. In response to Slave Sync, the IOC picks up the address, read, write, and word/byte information. It then removes Grant Sync.

5. The selected controller removes Slave Sync and the address, read, write, and word packing information.

A memory read transfer proceeds as follows:

1. The IOC requests memory access to the address specified in the selection sequence. When access is granted, the IOC acquires the content of the addressed memory location, and places either the entire word, or the byte specified by the selected controller, on the bus. If a byte, it is placed in the eight least significant bits.

2. The IOC activates the Memory Transaction signal on the bus and the S=4 action line (output). Then it activates Master Sync.

3. The selected controller picks up the data and activates Slave Sync.

4. The IOC removes Master Sync and the controller removes Slave Sync.

5. The IOC removes S=4, the data, and the Memory Transaction signal, and becomes ready for another transaction.

A memory write transfer proceeds as follows:

1. The IOC calls for data from the selected controller by activating the S=5 action line (input) and the Memory Transaction line. It then activates Master Sync.

2. The selected controller activates Slave Sync and places the data to be written in memory on the bus.

3. The IOC picks up the data and removes Master Sync. The selected controller then removes Slave Sync and the data.

4. The IOC removes S=5 and Memory Transaction and becomes not busy, ready for another bus transaction.

5. The IOC requests access to the memory location specified in the selection sequence. If a word transfer was specified, the request is for a memory write, and when granted, the data word is stored in memory, and this sequence is complete. If a byte transfer was specified, the request is for a memory read, and this sequence continues with Step 6.

6. When the memory read access is granted, the content of the addressed location is transferred to the IOC's holding register, and the byte specified in the selection sequence is replaced with the new data from the bus.

7. The IOC requests memory write access to the same location, and the modified word with its new byte is stored in memory.

4.5.5 GENIE I/O Bus Error Detection

The several types of errors that may be detected by controllers on the GENIE I/O Bus and by the GENIE I/O Bus controller are described in the following paragraphs. All such errors, except for a deadman timer error, are reflected back to the controller on the bus that is involved in the transaction, and the controllers normally store the error indication for testing by GEN 2 instruction JNE (see 4.5.2) The error indications are normally cleared by issuing an OPR instruction to the controller to initiate a new operation, by executing ABT addressed to the controller, or by pushing the Alarm/Reset button on the Programming and Maintenance Console. The indication may also be cleared by pushing the RESET/"O" pushbutton on the console while the console is enabled and in manual mode, thereby initializing the system hardware.

Data Parity

Controllers on the bus may check the parity of data received from the GENIE I/O Bus Controller (IOC), and may accept or reject data with incorrect parity, as deemed appropriate for each controller.

The IOC checks parity on all data received from controllers on the bus and reflects any detected errors back to the controllers. The data is transferred on to memory or the Arithmetic Unit, unchanged and regardless of the error.

The Memory Bus Controller generates a 6-bit error detection character for data written into memory and checks this character on data read from memory. The MBC can detect and correct any single bit error on memory read operations. 90% of all multiple bit errors or no response from the memory, will trigger an error indication.

Device Address

All controllers on the bus check device addresses for parity errors. If any are detected, all controllers should ignore the address information, and a deadman timeout should occur.

The IOC checks parity on all device addresses received from the controllers, and returns an error indication to the controller involved if such an error is detected. The IOC does not proceed with the transaction when such an error is detected.

Deadman Timer

Should a controller on the bus not return Slave Sync in response to Master Sync from the GENIE I/O Bus controller within a reasonable time, a deadman timer error indication is stored in the IOC which may be detected by JNE. See "25X74000 = JNE, Jump if No GENIE Bus Deadman Timer Error" under 4.5.2.

4.5.6 Bus Extension and Switching

The extension of the Master Bus to a 16-load Slave Bus and the switching of a Slave Bus between two, three, or four Central Processors is accomplished by the AXES11 Bus Extender Switch (see Fig. 4-4). The extension of the Master Bus via Slave Busses for one CPU is accomplished via the Bus Extender Only, AXBE11. Hereinafter, the Bus Extender and Bus Extender Switch options are refered to as the Bus Extender/Switch. The Bus Extender/Switch is an addressable controller on the GENIE Bus that uses one of the available 256 device addresses, as selected on each Extender/Switch board. The Bus Extender/Switch also has API priority selection switches that select its API priority relative to other modules on its Master Bus. The Bus Extender/Switch's API priority is the same as the priority of the Slave Bus it creates, relative to other Slave Busses on the Master Bus. Therefore, the priorities of the two API's generated by the Bus Extender/Switch have the first two priorities out of the 32 possible interrupts generated by the Bus Extender/Switch and the 15 possible controllers on the Slave Bus.

Bus Extender/Switch Controls and Indicators:

Address Selection Switches; these select the address (DDC) of the Bus Extender/Switch, which may be any available address not used by another controller to be addressed from the same Central Processor.

Priority Switches; these select the relative priority of the Slave Bus segment created by the Bus Extender/Switch relative to other controllers on the Master Bus. These switches also determine the relative priority of the two API's generated by the Bus Extender/Switch.

Request Local/Remote Switch; when the Slave Bus is common to more than one Central Processor, access to the Slave Bus is controlled by the Central Processors when this switch is in the Remote position. When placed in the Local position, it generates an API that requests the program in the associated Central Processor to place the Bus Extender/Switch in Local mode.

Local Select/De-Select Switch; after the associated CPU has placed the Bus Extender/Switch in Local mode, this switch selects the Bus Extender/Switch to connect the Slave Bus to the Master Bus, or it de-selects it to disconnect the Slave Bus from the Master Bus.

Force Local/Remote Switch; this switch forces the Bus Extender/Switch to Local mode in the event that the CPU did not respond to the request generated by the Local/Remote switch. This method for local control of the select/de-select condition of the switch is not normally used, and should be used only if the Slave Bus can be safely de-selected. The Busy and Select indicators indicate the traffic through the Bus Extender/Switch. Manual Override should be selected only when there is no traffic.

Extender Switch/Extender Only Pin; if the Bus Extender/Switch is one of 2, 3, or 4, such modules used to create a Slave Bus that is common to more than one Central Processor, this Jumper Pin is placed in the Extender Switch position. If a single Central Processor is connected to a Slave Bus dedicated to it, this Jumper Pin is placed in the Extender Only position.

De-select/Do Not De-select; inhibits the CPU from de-selecting the Slave Bus from the Master Bus when this pin is placed in the Do Not De-select position. When placed in the De-select position allows the Bus Extender/Switch to operate normally as a switch.

4400/4500 Pin; conditions the Bus Extender/Switch to function with the selected system, either a 4400 or a 4500.

Common Power OK Indicator; indicates that +5 Vdc power is on the Slave Bus.

Common Selected Indicator; when on, the Bus Extender/Switch is selected and its Slave Bus is connected through to the Master Bus.

Local Granted Indicator; when on, the CPU has answered a request for Local mode and the Bus Extender/Switch can be selected or de-selected manually.

Common Bus Busy Indicator; traffic through the Bus Extender/Switch illuminates this indicator, and its intensity is an indication of the volume of traffic.

CPU Alarm Indicator; indicates that an error condition has been detected by the Bus Extender/Switch or it's Slave Bus. These error conditions are either a parity error or a power failure.

Interrupts

The first API generated by the Bus Extender/Switch (type 0, see 4.3) is an alarm interrupt which indicates that the program should read the status of the Bus Extender/Switch.

The type 0 API is non-inhibitable, is normally serviced by an SPB instruction in the API response location, and occurs when logic power fails on the Slave Bus or an "external alarm" (stall or parity alarm) has been detected by one of the Bus Extender/Switches on a Common Slave Bus. The second API (type 1) is generated when the Local/Remote switch is set to Local, to request Local mode. The type 1 interrupt is inhibitable and is normally serviced by an SPB instruction in the API response location.

GEN 2 Instructions

The following GEN 2 instructions, when addressed to a Bus Extender/Switch, affect it as described:

IN S'=1; (Also defined as IDS - Interrogate Device Status). This instruction transfers the status of the Bus Extender/Switch to the A Register in the AU. The status word is defined on Fig. 4-5.

OPR S'=0; if the Slave Bus is available through the addressed Bus Extender/Switch, OPR selects that Bus Extender/Switch, connecting the Slave Bus through to the Master Bus. If the Slave Bus is not available, as indicated by the status word, OPR is ignored.

ABT S'=0; this instruction de-selects the addressed Bus Extender/Switch, disconnecting the Slave Bus from the Master Bus. If it is in Local mode or is already de-selected, ABT is ignored.

ACT S'=0; this instruction is the CPU's answer to an API or status word requesting Local mode, and places the Bus Extender/Switch in Local mode. If the Remote/Local switch is in Remote, ACT is ignored.

4.6 POWER FAIL RESTART

Power interruptions shorter than 30 ms have no effect and are ignored by the TDC 4500. Power loss beyond this time will trigger the Power Fail interrupt (location 200_8). This interrupt gives the system 1 ms warning that power is out of limits and may fail. A program should switch to a routine which will allow an orderly shut down. If the Memory Battery Backup option is present, data stored in MOS memory will be saved for at least 15 minutes (memory locations 0-10 are hardware registers and are not preserved). When power returns, and if the Programming and Maintenance Console is disabled, the internal firmware checks to see if MOS memory power stayed on. If so, the memory contents are valid. Sequencing then resumes with the instruction in trap location 22_8.

If MOS memory power was lost during the power failure, and if the console is disabled, the Auto Reboot freature will try to reload main memory from bulk storage (if present). It does this by moving a bootstrap routine into the top of main memory and branching to it. The bootstrap will load the first 100_8 locations into main memory from the bootstrap section of unit 0 on GENIE Bus device 40004_8*. The bootstraps transfer control to memory location 0, where a routine reloads the main memory from bulk.

In either case, if the Programming and Maintenance Console was enabled the processor will power up in the "Halt" mode. An indicator on the Battery Backup option will show whether or not MOS memory power stayed on during the outage. An operator may then use the RESET and KEY-BOARD switches to select a program load source or resume sequencing.

4.7 CSU POWER SYSTEM

Ac power input to the TDC 4500 is 104-127 Vac at 47-63 Hz. Other voltages such as 220 V, 50 Hz may be used if applied through a suitable transformer. Maximum input surge current is less than 300% of normal operating current. The CSU power system contains a power entry panel, ac and dc power distribution wiring and up to three power chassis.

The First Power Supply chassis provides basic logic and memory voltages. It also supplies 12 Vac for the Line Frequency Clock and 24 volts for sequencing and control. Logic voltages (+5, +15 Vdc) and MOS memory voltages (+5, +12 Vdc) are protected by overvoltage, overcurrent, and overtemperature monitors. 28 volt peripheral power is adequate to operate two card readers and one card punch. The processor chassis, MOS memory, and First I/O chassis are powered from the First Power chassis.

*4500B processor will try to load from address 4004_8, then revert to address 4005_8 if necessary, as described in part 4.1.5. Any secondary bulk memory device used on address 4005_8 must, of course, be suitably prepared to supply the program needed for system recovery. The Floppy Disc isn't recommended for Auto-Bootstrap use.

The Second Power chassis or Expansion Power chassis is added to furnish logic voltages and 28 volt peripheral power for up to three additional GENIE Bus chassis. Both chassis types contain a high efficiency switcher type power supply. Sequenced ac power to both the First and Second Power chassis is turned on and off by a switch on the Programming and Maintenance Console.

4.7.1 MOS Memory Battery Backup Chassis

When the ABBU11 Battery Backup option is present, it supplies MOS memory power (+5, +12 Vdc) and stays on even when the console On/Off switch has shut off the other power supplies. If ac power fails, power is supplied to the MOS memory (without interruption) from three "gelled-electrolyte" batteries. These batteries are sealed and require no maintenance. They will sustain 256 k of MOS memory for at least 15 minutes (longer for smaller memories). If the batteries are discharged below a safe level, they are automatically disconnected. An internal battery charger restores the batteries and keeps them charged. Battery life is estimated at four to five years. A panel indicator remains on so long as adequate voltage is supplied to the MOS memory (thus preserving the contents of memory). If memory power is actually lost, the indicator turns off (before control power is lost) and stays off until manually reset even though ac power returns. The processor's firmware also senses a "memory voltage valid" signal and adjusts its power fail restart routine accordingly (see 4.6).

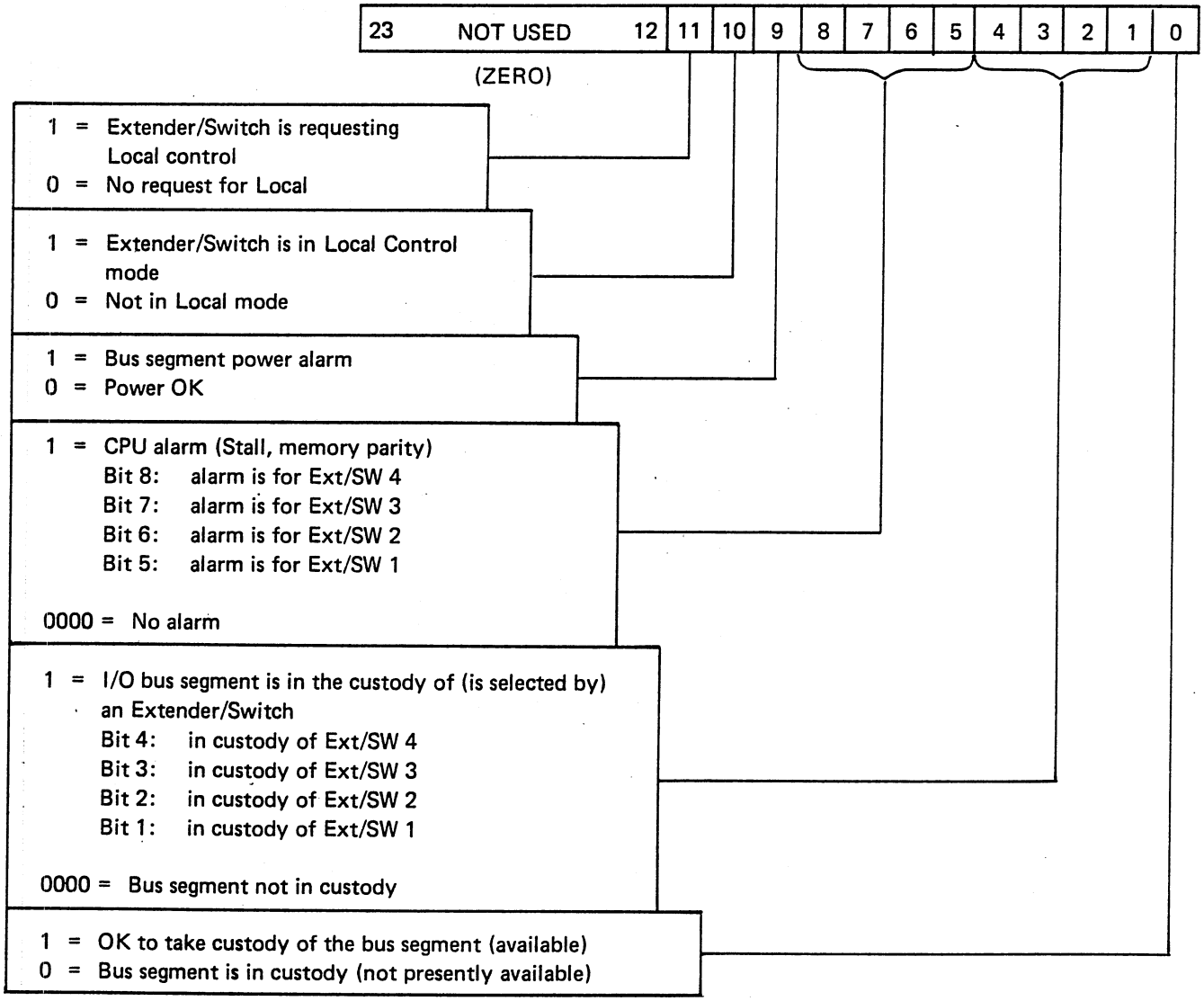


Fig. 4-5 Bus Extender/Switch Status Word

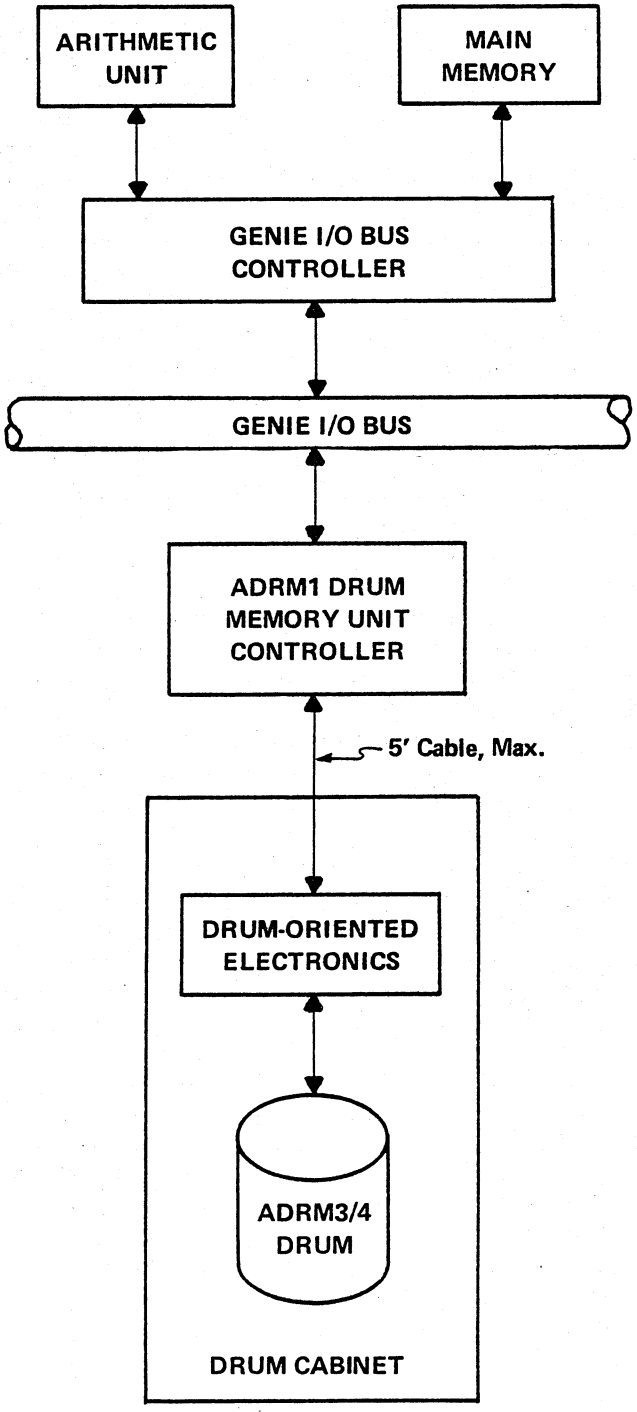


Fig. 5-1 Drum Memory Subsystem

DRUM MEMORY

Drum memory provides a large, reliable, economical, fast, random-access bulk storage medium for real-time programs and data that are transferred to and from main memory as needed by the running program. The data is magnetically recorded on a rotating cylindrical drum by fixed-position heads, each of which flies just above the track on the drum surface on which it writes information and from which it reads information. Information recorded on the drum is retained on the drum when transferred to main memory and may be altered when rewritten under control of the program. A Drum Memory Subsystem configuration is depicted on Fig. 5-1.

5.1 FUNCTIONAL DESCRIPTION

Data are recorded on the drum in tracks of 40 sectors, with 64 24-bit data words in each sector - a total of 2560 data words per track. Each 24-bit data word is the image of the corresponding word in main memory at the time the word was written on the drum. Each sector also includes a preamble, a header, a polynomial check segment, and a postamble, as shown at the top of Fig. 5-2. These are all recorded each time a sector is written. The polynomial check segment contains a unique check pattern which is representative of the information in the sector. Thus, if any word in the sector is to be rewritten, the entire sector must be rewritten. As a sector is read, the check segment pattern is checked against a pattern regenerated while reading the information in the sector. The minimum transfer length, therefore, is one 64-word sector and all transfers must be integral multiples of sectors, up to a maximum of 255 sectors (16,320 words).

The storage capacity of the drum is a function of the drum shell size and the number of heads installed. The largest available drum can store up to 1,310,720 words (see 5.2 Options). Each drum cabinet includes the power supplies and electronics necessary to support the drum and can accommodate one drum up to the largest capacity.

The drum cabinet's interface with the Central Processor is through a drum controller on the GENIE I/O Bus, which is controlled by GEN 2 instructions issued by the program (5.4.2) and exchanges data with main memory through the GENIE Bus Direct Memory Access port (4.5.4). The Drum Memory Subsystem is capable of accessing any location in dedicated memory within 262,144 words.

5.2 OPTIONS

5.2.1 Drum Memory Unit Controller Options

The drum controller on the GENIE I/O Bus has device address and interrupt priority selection controls on the printed wire boards that permit selection of any of the available 256 GENIE Bus device addresses, and any of 15 API and direct to memory request priorities that are subsidiary to the priority (1 of 16) of the Slave Bus on which the controller is installed. If the controller is on a Master Bus section, one of the 16 Master Bus priorities is selected. (See 4.5 and Fig. 4-4.) Device address 404_8 must be selected for the drum controller serving a drum to be used as a bulk program load device.

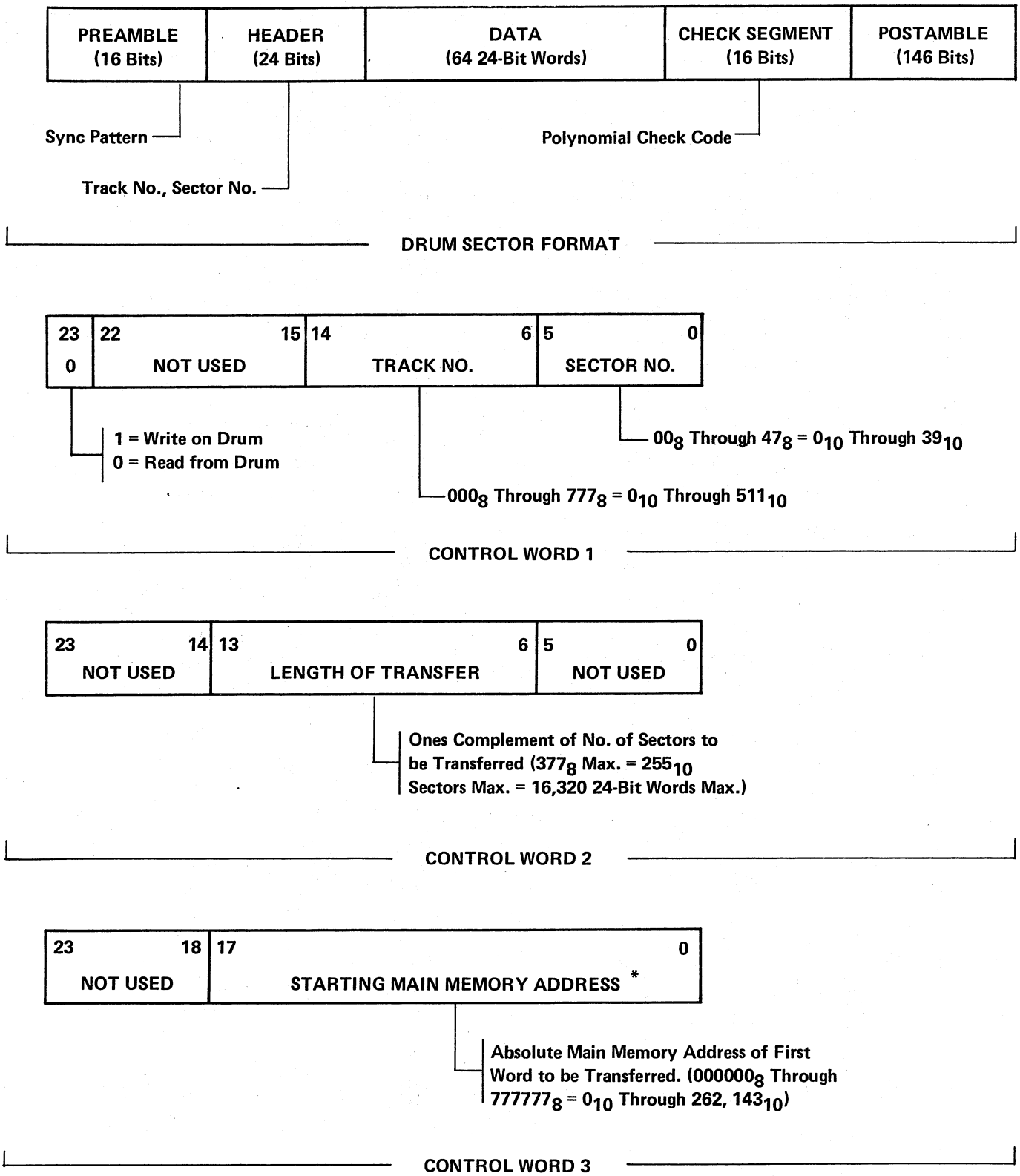
5.2.2 Drum Options

All of the drums shown in Table 5-1 have a 512-track shell which can accommodate up to 1,310,720 words. Drums implementing less than the full head capacity can be expanded in the increments indicated below, but the installation must be accomplished in a controlled environment. Arrangements can normally be made to use an exchange drum while a drum is expanded.

The drums are available in a pressurized enclosure for operation in environmental class A.

Drums are available to operate on 60 Hz power or on 50 Hz power. See 3.2.2.

Available option combinations are listed on Table 5-1.



*Due to the "look ahead" operation of the Drum Controller, an attempt to read from the last 64 words of implemented memory on a TDC 4500 process computer, and to write that information ona a drum, results in a blue error.

The user may either ignore the blue error and recover from it or refrain from the use of the last 64 memory words for transfer to the drum.

Fig. 5-2 Drum Sector and Control Word Formats

MODEL	WORDS IMPLEMENTED	LINE FREQUENCY
ADRM31	327,680	60 Hz
ADRM45	327,680	50 Hz
ADRM32	655,360	60 Hz
ADRM46	655,360	50 Hz
ADRM33	983,040	60 Hz
ADRM47	983,040	50 Hz
ADRM34	1,310,720	60 Hz
ADRM48	1,310,720	50 Hz

Table 5-1 Drum Options

5.3 PRINCIPAL FEATURES

5.3.1 Latency Time

Latency time is the time from the program's initiation of a drum transfer until the addressed sector on the selected drum track is found, so that the data transfer can begin. This is a function of the drum rotating speed and for drums operating on 60 Hz power, the average latency time is 8.7 ms, and the maximum latency time is 17.4 ms. For drums operating on 50 Hz power, the average latency time is 10.4 ms and the maximum latency time is 20.8 ms.

5.3.2 Start-Up Time

The drum is up to speed and ready for operation within four minutes from the time power is applied to the motor. However, to assure operation equal to or exceeding the accuracy specifications (5.5.3), the drum should be allowed to warm up for 15 minutes if started at an ambient temperature between 15°C and 50°C. One hour of warm-up time should be allowed if the drum is started at an ambient temperature between 0°C and 15°C.

5.3.3 Accuracy

The recoverable error rate for transfers to and from the drum does not exceed one bit in 10^{11} bits transferred, where a recoverable error is one which can be overcome by accomplishing an error-free transfer within three attempts. The non-recoverable error rate does not exceed one bit in 10^{14} bits.

5.3.4 Transfer Rate

The average transfer rate for multiple sector transfers is approximately 147,000 words per second for drums operating on 60 Hz power, and for drums operating on 50 Hz power, it is approximately 122,880 words per second.

5.3.5 Write Protection

A Write Protect selection panel is provided on the drum unit. It is accessible when the cabinet door is open. Switches on that panel may be used to select 4-track blocks (10,240 words) in the first 32 tracks (81,920 words), and 16-track blocks (40,960 words) for the next 224 tracks, and 128-track blocks (327,680 words) for the balance of the implemented tracks, for protection from inadvertent writing on the selected tracks. When an attempt is made to write on a protected track, a write protect alarm indication is stored in the Alarm Register (5.4.4).

5.3.6 Transferred Data Validity Verification

Each drum sector (Fig. 5-2) contains a polynomial check segment that contains a unique pattern that is representative of the track number and sector number contained in the header plus the 64 data words. The check segment is generated by the hardware and recorded as the sector is written. The pattern is regenerated by the hardware as the sector is read, and it is compared with the recorded pattern. If they do not compare, a Data Check Alarm (see 5.4.4) is generated. The GENIE Bus data and address parity checking described under 4.5.5 also apply to the Drum Memory subsystem.

5.3.7 Power Failure Protection

Data recorded on the drum is protected from alteration during power failures or deliberate shutdowns. It is also protected when power is reapplied. Should a power failure occur during a read from the drum transfer, the Drum Memory Subsystem may sequence off before reading of the sector is completed. Should a power failure occur during a write on the drum transfer, the integrity of the data and the polynomial check segment may be destroyed. Any transfer interrupted by a power interruption should be reinitiated. If the drum has slowed below its minimum operating speed, it may be necessary to wait for it to resume speed, as indicated by the DU alarm status bit (5.4.4). A successful one-sector read transfer will verify that proper operation is reestablished.

5.4 OPERATING SEQUENCE

The parameters of a drum transfer are specified by the three control words shown on Fig. 5-2. The control words are transferred to the drum controller by GEN 2 instructions (5.4.2). Control Word 1, which specifies the starting address on the drum, is transferred from the A Register by an OPR S'=0 instruction addressed to the drum controller. The OPR S'=0 instruction also initiates the actual transfer. Prior to execution of OPR S'=0, Control Word 2, specifying the length of the transfer, and Control Word 3, specifying the starting main memory address, must have been transferred to the drum controller. These two words are transferred from the A Register by OUT S'=0 and OUT S'=1, respectively.

5.4.1 Transfer Sequence

The sequence of events in a typical drum transfer is as follows:

1. The program transfers Control Word 2 and Control Word 3 to the drum controller by placing each word in the A Register and then executing the appropriate OUT instruction. OUT S'=0 indicates that the word is CW2. OUT S'=1 indicates that the word is CW3. They may be issued in any order and at any time prior to initiation of the transfer. CW2 is the starting sector address in complemented form (377_8 specifies zero sectors and 000_8 specifies 255 sectors)

2. The program places Control Word 1 in the A Register and executes OPR S'=0 addressed to the drum controller.

3. The controller goes "not ready", selects the head specified by the track number specified by CW1, and when the starting sector passes under the head, the transfer begins. As the transfer proceeds, the controller makes necessary main memory requests, updates the main memory and drum addresses, and increments the transfer length count as each full sector is transferred.

4. When the transfer is completed, the drum controller goes "ready" and requests a transfer complete API (5.4.3). The program may then verify that the transfer was error free by executing JNE addressed to the controller.

Should an ABT S'=0 instruction be issued to the drum controller (5.4.2), or should an error be detected during a transfer (5.4.4), the transfer is completed prematurely, the controller goes "ready", and a transfer complete API (5.4.3) is requested.

Should CW2 specify a transfer of zero sectors, the drum controller goes "not ready" when OPR is executed, and then "ready", a transfer complete API is requested (5.4.3), and no transfer takes place.

5.4.2 GEN 2 Instructions

The following GEN 2 instructions addressed to the drum controller affect the Drum Memory Subsystem as described (refer also to 4.5.2):

ABT S'=0; Conditional Abort. This instruction initiates an orderly termination of any drum controller operation to free the controller for alternate operations. Any operation in progress is terminated as soon as possible without disrupting the integrity of any data movement in progress. If data movement is in progress, the transfer is completed at the end of the current sector.

ABT S'=1; Unconditional Abort. This instruction immediately and unconditionally initializes the drum controller. It is intended for use in troubleshooting and by test and diagnostic programs, and is not normally used by on-line programs.

ACT; Activate Interrupt. ACT S'=0 activates the transfer complete interrupt and ACT S'=1 activates the unit ready interrupt (see 5.4.3).

AIM; Activate Interrupt Mask. This instruction masks the drum controller transfer complete and unit ready interrupt requests (5.4.3).

DIM; Deactivate Interrupt Mask. This instruction unmasks the transfer-complete and unit-ready interrupt requests if they were masked by the AIM instruction.

IN; Input. IN allows the program to read the contents of the principal drum controller registers at any time, whether a transfer is in progress or not. If a transfer is in progress or has been completed, the CW1, CW2, and CW3 registers reflect the updating that has taken place since they were set up prior to the transfer. The S' digit in the instruction word indicates which register's contents are to be transferred to the A Register ——

S' = 0 = Alarm Status Register (5.4.4)

S' = 1 = Control Word 1 Register

S' = 2 = Control Word 2 Register

S' = 3 = Control Word 3 Register

JNE; Jump if No Error. This instruction tests the status of the drum controller alarm indicator which is set if any alarm bit in the Alarm Status Register is set (5.4.4).

JNR; Jump if Not Ready. JNR tests the status of the drum controller "ready" line. The controller is "not ready" from the time a transfer is initiated by OPR until the transfer is complete or terminated prematurely.

OPR; Operate. OPR S' = 0 transfers the contents of the A Register (CW1) to the drum controller and initiates a transfer. CW2 and CW3 should be transferred prior to interrupt request (5.4.3) and no other action is taken.

OUT; Output. OUT S' = 0 transfers Control Word 2 to the drum controller and OUT S' = 1 transfers Control Word 3 to the controller. See 5.4.1.

5.4.3 Automatic Program Interrupts

At the completion of a drum transfer or the premature termination of a transfer, the drum controller requests a transfer complete (Drum Memory Subsystem ready) API. The controller also makes a unit ready (RTZ) API request when a zero length transfer is requested (5.4.1). The unit ready API is provided to preserve a degree of compatibility with programs designed for the dual bulk controller which is used on earlier process computer systems.

Both API's are inhibitable (4.3.3). The transfer complete API has the higher priority of the two and is the first of the two consecutive interrupt response addresses (4.3.1).

The transfer complete API may also be triggered by ACT S' = 0. The unit ready API may also be triggered by ACT S' = 1 or by OPR S' = 1.

5.4.4 Alarm Detection

The Drum Memory Subsystem hardware detects six alarm conditions that indicate improper hardware or software operation or the inoperability of the hardware. These conditions are indicated by the Alarm Status Register (Fig. 5-3). When any of the alarm conditions is detected, the drum controller's alarm line, which may be tested by GEN 2 instruction JNE, is set. The Alarm Register may also be transferred to the A Register in the Arithmetic Unit by GEN 2 instruction IN S' = 0. If an alarm is detected while data movement is in progress, the transfer is completed at the end of the current sector.

The Alarm Register bits and the alarm line are reset (with the possible exception of the DU alarm) when a new transfer is initiated by OPR S' = 0, by the ABT instructions, when the Alarm/Clear button on the Programming and Maintenance Console is pushed, or when the system hardware is initialized.

The alarm conditions are as follows:

Data Check Alarm (DC) (Bit 0). A GENIE I/O Bus parity error has been detected (4.5.5), or on reading from the drum, the polynomial check segment read from the drum did not compare with the check pattern regenerated as the sector was read. If a parity error was detected on the transfer of a control word to the controller, the transfer cannot be initiated until the control word is successfully retransferred. If the alarm occurs while writing on the drum, writing continues to the end of the sector, but the controller writes fill words in the remainder of the sector. If the alarm is due to an incorrect comparison of the check segment, the transfer terminates at that point, which is the end of the sector.

Drum Unsafe (DU) (Bit 1). The drum is not up to minimum operating speed, the heads are not flying over the drum surface, the drum power supply is out of tolerance, or both read and write control signals are applied to the drum at the same time. These conditions are due to an ac power failure, not allowing sufficient time for the drum to come up to speed, or a hardware failure.

Drum Address Limit (DL) (Bit 2). The drum address specified by the controller exceeded the highest address implemented on the drum. This could be due to an incorrect Control Word 1, a transfer beginning at an implemented address but continuing beyond the highest implemented address, or a hardware failure.

Address Comparison Alarm (AC) (Bit 3). On a read from the drum transfer, the address read from the sector

header did not compare with the address in the drum controller's drum address (CW1) Register. As transfers proceed, the address register is incremented as each sector boundary passes the selected head. If the address read from a sector does not compare with the controller's address register, either an incorrect first sector for a transfer was found, or during the transfer, the controller and the drum did not maintain the same sector sequence.

Write Protect Alarm (WP) (Bit 5). An attempt was made to write on a drum track protected by the Write Protect selection switches (5.3.5). This can be due to a software error, incorrect selection of a Write Protect switch, or a hardware malfunction.

Memory Timing Alarm (MT) (Bit 8). A request for main memory access was not honored before a data word read from the drum was replaced by a new word read from the drum, or was not honored in time to provide a new word to be written on the drum. This alarm could occur because of a hardware malfunction or because DMA activity on the GENIE Bus is so high that the memory data bandwidth of the bus is exceeded. The bus memory data bandwidth could be exceeded due to a large number of devices on the bus with DMA capability and the occurrence of a period of high DMA demand.

5.5 ADDITIONAL DRUM SUBSYSTEM CHARACTERISTICS

5.5.1 Primary Drum Cabinet Power

See 3.2.4 in Section 3 of this General Description.

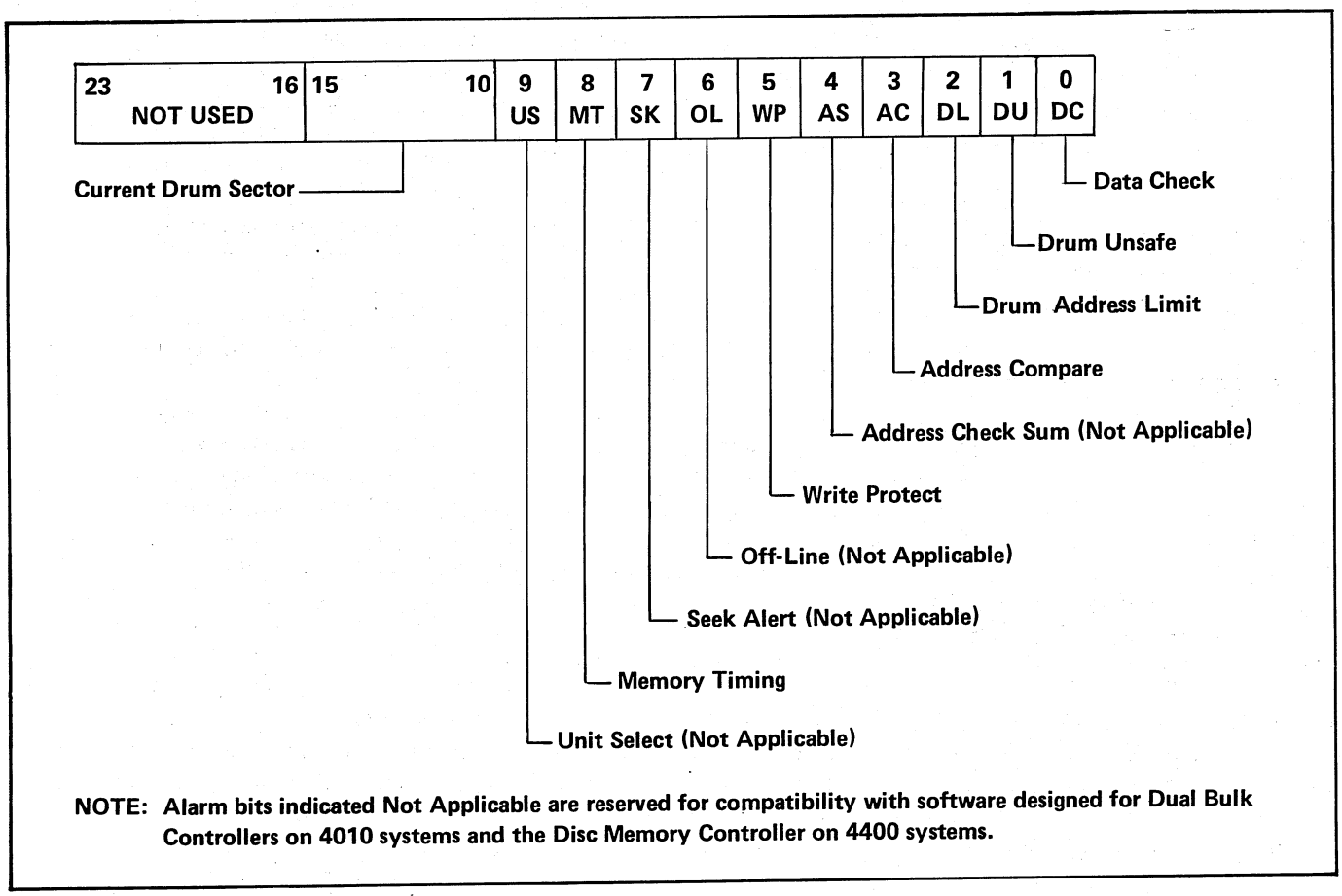
5.5.2 Drum Cabinet Physical Characteristics

The drum cabinet is 30" wide, 76" high, and 32" deep. With the largest drum installed, the cabinet weighs approximately 520 lbs.

5.5.3 Environmental Classes

The ADRM1 Drum Controller is normally in environmental class A. See 3.1 and Table 3-1.

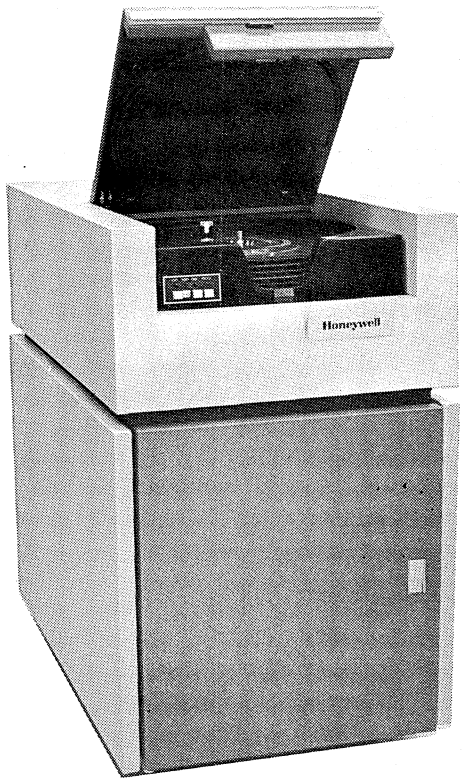
The drum unit and associated components in the drum cabinet are in environmental class A.



NOTE: Alarm bits indicated Not Applicable are reserved for compatibility with software designed for Dual Bulk Controllers on 4010 systems and the Disc Memory Controller on 4400 systems.

Fig. 5-3 Alarm Status Register

MOVING HEAD DISC SUBSYSTEM



The Moving Head Disc Subsystem provides bulk storage of over 67 million words, accessible on line using standard TDC 4500 software packages. Transfers take advantage of the system's direct-to-memory access capability and feature a new, multi-request queue function that optimizes disc transfer requests, minimizes head movements and maximizes data throughput.

Up to four 8-million word disc units can be accommodated on each disc subsystem. Standard software may access an additional 8-million words on each disc unit by treating this area as an additional logical mass storage unit. Standard software supports up to eight logical mass storage units on each computer system, of which four such units may be used for program storage.

6.1 FUNCTIONAL DESCRIPTION

Fig. 6-1 illustrates the functional configuration of the Moving Head Disc Subsystem. Data transfers occur between Memory and the disc units as depicted in the diagram. The GENIE Bus Controller (GBC), described in detail in a previous section, is the communications link for the Bulk Memory Controller (BMC) in its information exchanges with the Processor and Memory. The BMC services requests from the Processor for the data transfers. An adapter subcontroller provides the communication link between the BMC and the disc units.

All transfers are initiated by user calls to the RTMOS operating system. Standard RTMOS driver routines set up the transfer requests using control words placed in a queue table in memory and then request BMC action using a pointer word request. The BMC services the requests, accessing the control words as necessary to perform the transfer operations and support functions.

Support functions provided by the BMC include optimization of head movements and sector rotations, error checking and corrections, automatic retry for recoverable errors, data buffering, and program communication (status and interrupt).

6.2 OPTIONS

NOTE

This description defines the operation of both "A" version (wire-wrap) and "B" version (copper) MHD Subsystems.

Model Numbers

There are two versions of the Moving Head Disc Subsystems. The first is designated as the "A" version, while its sucessor is designated as the "B" version. There are some minor functional differences between the two, such as request queue size, maximum record transfer size, plus a few new functions (Data Recovery control on Read operations and a Compare Data operation) with the "B" version not found in the "A" version. (The "B" version does have the capability to be program selected for compatibility with the "A" version, but the "B" version is primarily intended as an expanded capability subsystem. The expanded capability refers to the BMC portion of the subsystem, which is designed for multiple device type handling - such as disc, mag tape, and inter-system link communications.)

The most distinguishing differences between the "A" and "B" versions of the MHD Subsystem are the physical characteristics of the Bulk Memory Controller. The "A" version of the BMC uses wire-wrap version PWAs (Printed Wiring Assemblies), each of which required two card slots in an I/O Chassis. The "B" version uses copper PWAs which only require single card slots for each board.

The model numbers for the "A" and "B" versions of the MHD Subsystem are as follows:

- Controller (BMC) - 4DP3BABMC101-104 ("B" version, ported)
  - 4DP3AABMC101-101 ("A" version)
- Moving Head Disc - 4DPAADSC301-302
- Disc Pack - 4DP3AADSC401
- Disc Cable Sets - 4DP3AAZDS102&105
- Bulk Memory Sub-Controller - 4DP3AABMS102&104

BMC Controller GENIE Bus Address

Like all standard controllers connected on the GENIE Bus, the BMC contains switch-selectable address and priority options that permit reconfigurable address and priority of the BMC on the I/O Bus.

6.3 PRINCIPAL FEATURES

6.3.1 Latency Time

Latency time is the time from the program's initiation of a disc transfer until the addressed sector can be read or recorded by the addressed head. The average latency time, where no head movement to a cylinder is required, is 8.6 milliseconds (½ revolution of disc), and the maximum latency time with no head movement is 17.2 milliseconds (full revolution). Head movements add 6 milliseconds for a one track movement, and 30 milliseconds for a full 409 track movement.

6.3.2 Start-up Time

The disc pack is up to speed and ready for use approximately 30 seconds after power is applied to the unit.

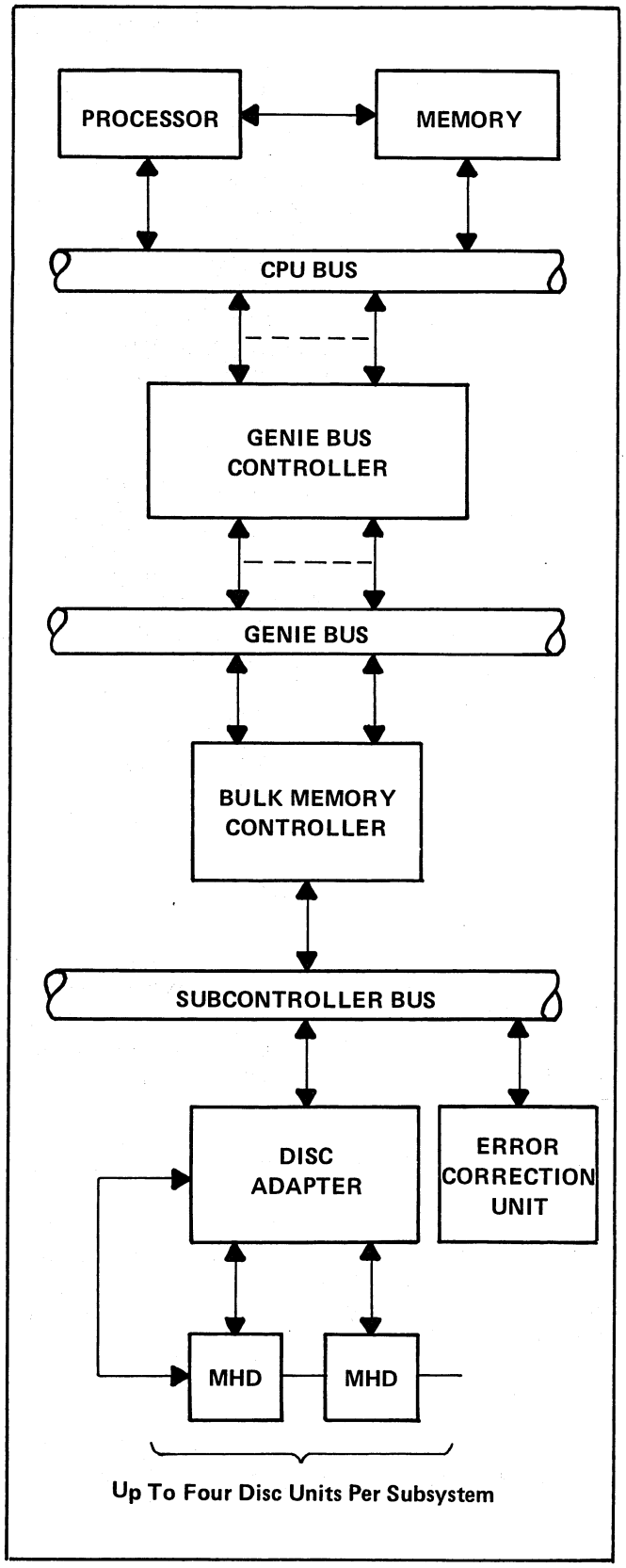


Fig. 6-1 Organizational Block Diagram - Moving Head Disc Subsystem

6.3.3 Transfer Rate/Size

The transfer rates of information exchanges are as follows:

- Sector burst - Disc to BMC:
  390,694 words per second

  BMC to memory:
  250,000 words per second

- Whole track average:
  238,139 words per second

The maximum size of record transfers are as follows:

- "A" version - $16{,}230_{10}$
- "B" version - $262{,}144_{10}$

6.3.3.1 Data Buffering

The average data transfer rate for the MHD subsystem is nearly equal to that of the I/O Bus. To prevent overruns when the bus controller is tied up in other transfers and cannot immediately service MHD transfers, a data buffer in the BMC holds up to two sectors of data.

On read operations from memory, the BMC's data buffer holds data written on the disc. On write-to-memory operations the buffer holds data read from the disc. During write-to-memory operations the BMC will not read another sector until there is enough room in its buffer to hold a complete sector. Should the bus be busy during an entire sector, the BMC lets the disc rotate one entire revolution and then performs the transfer, 18 milliseconds later. When reading from memory, the BMC will not start to write a sector until the data is in its internal buffer.

6.3.4 Write Protection

Two forms of write protection are incorporated in this subsystem: by entire unit or by sector within a unit.

Unit write protect is enabled by activating a Write Protect switch at the unit.

Sector write protection is enabled by the writing of a protect bit at the sector's header information during a write header operation. This protection remains unless altered under program control with a Write Header operation. The Format Write switch must be activated when writing sector format (header) information on the disc pack.

6.3.5 Data Validity and Recovery Techniques

Transfers between the GENIE Bus Controller and the BMC are parity checked. In addition, data written on the disc packs contain an EDAC (Error Detection and Correction) code that is checked when the information is retrieved. The EDAC code provides information sufficient to detect bit losses of up to 22-bit bursts and to correct burst losses of up to 11-bits. The BMC automatically makes three attempts to recover data that is non-correctable and notifies the operating system of any recoverable and/or non-recoverable errors.

6.3.6 Power Fail/Auto Restart

Data recorded on the disc pack is protected from alteration during power failures or deliberate shutdowns. It is also protected when power is reapplied. Any transfer interrupted by a power disruption should be reinitiated. If the disc pack has slowed below its minimum operating speed, as indicated by a corresponding error code in the termination status portion of the entry table after the transfer, it may be necessary to retry the operation until the disc resumes speed. (The disc requires a maximum of 30 seconds to reach operational speed.) A successful one-sector read transfer will verify that proper operation is reestablished.

6.3.7 Head and Sector Optimization

The disc subsystem includes the capability to optimize transfers on the basis of both sector rotation and head movement.

For head optimization, the MHD subsystem processes requests in an order that keeps the read/write heads moving in a constant direction. The next request serviced is the request whose cylinder address is in the current direction and is closest to the cylinder address where the disc read/write head presently resides. When there are no requests remaining in the request queue of the disc in the current direction, the direction of the disc read/write head is reversed and the process continues.

For sector optimization, the next request serviced is the request whose sector is forward and closest to the sector that is presently under the read/write heads.

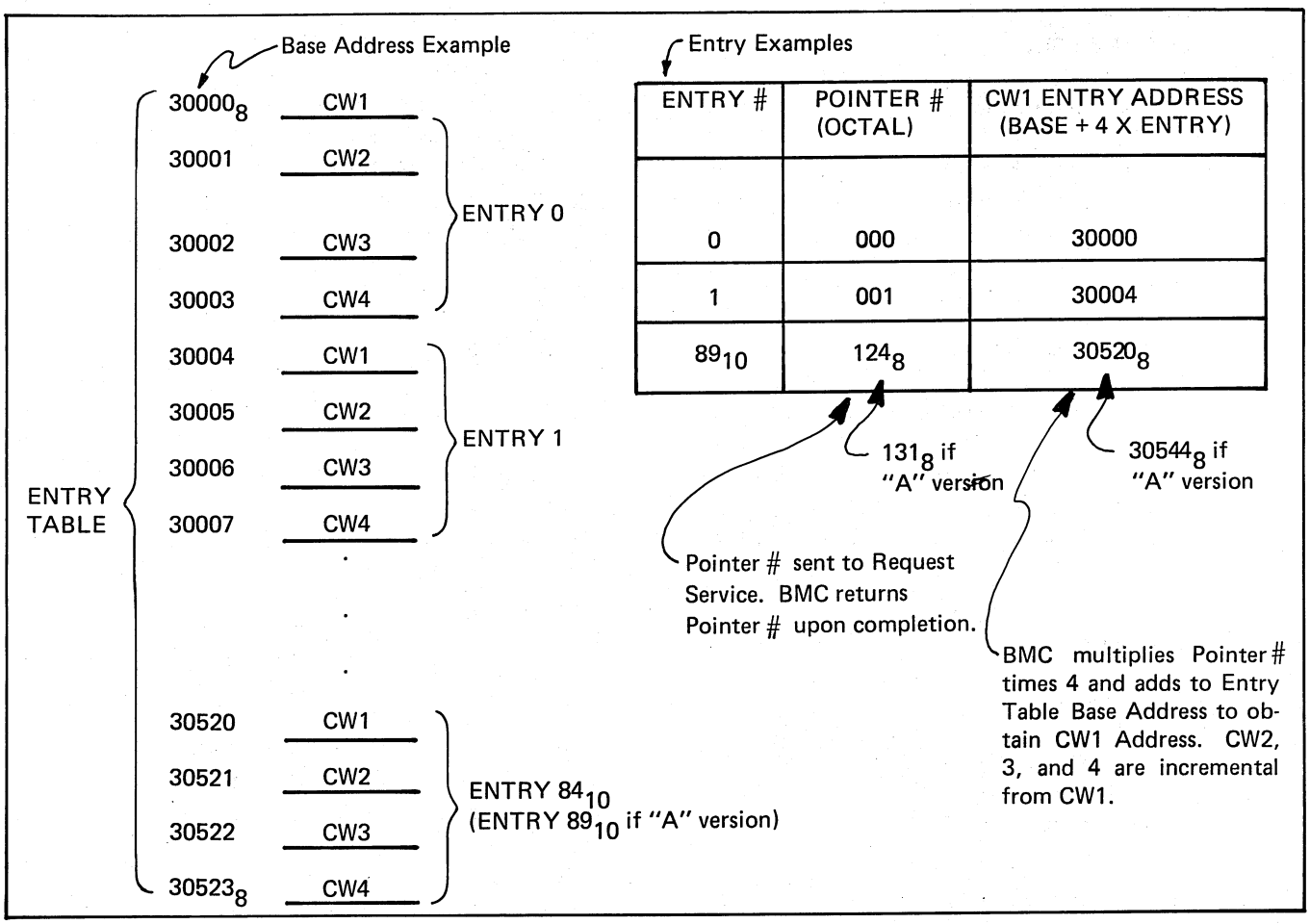


Table 6-1 Entry No./Pointer No./Table Addressing Examples

6.4 OPERATING SEQUENCE

The servicing sequence for operations requested of the MHD subsystem involves interaction between the processor, BMC, and an entry table in Memory.

Prior to initiating a request for BMC service, the processor sets up control words in the entry table. These control words specify the parameters (i.e., transfer direction, transfer length, starting addresses, etc.) for the operation to be performed. The actual operation is then requested using a GEN 2 OUT command to transfer a pointer number (representing the entry number of the request) to the BMC. (Refer to Table 6-1 for an example of the entry and pointer number calculations.) The BMC optimizes the transfers on the basis of disc head movements and disc rotation. Upon completion of a request, the BMC writes a termination status in the corresponding control word in the entry table and then interrupts the processor to indicate transfer completion. The processor responds with an IN command that reads in the pointer number of the completed control word group.

There are eight unique functions that can be requested for BMC servicing. The functions, separated into three basis categories for description, are as follows:

1. Data Transfers (Read Data, Write Data Compare, Write Data Skewed)
2. Header Transfers (Erase and Write Header, Read Header)
3. Control and Test (Entry Abort, Reset, Read Characteristics)

Unless specified as immediate operations, all data and header transfers are optimized. If immediate response is indicated (bit 16 set in CW4 of entry), the BMC responds immediately to the request, rather than servicing it on an optimized basis. (Read Characteristics, Reset, and Cancel requests are always regarded as immediate operations.

6.4.1 BMC Setup

There are setup operations that must be performed on the BMC prior to initiating transfer requests. These operations are sent at system initialization. They are:

1. Loading Entry Table Starting Address
2. Placing BMC in "Normal" mode

The BMC will remain in the "normal" mode until addressed with a subsequent ABT command or System Reset. (Refer to the OPR S' coding descriptions under the Program Control heading in this section to determine the function of the various mode selections.) The Entry Table Starting Address will remain unless power is lost to the BMC.

6.4.2 Data Transfer Operations

Table 6-2 is a summary of the functions required for a data transfer (Read Data/Write Data/Write Data Skewed, and Compare Data - if "B" version) operation. Note that the functions labeled "Prior to Transfers" are required only at system initialization to set up the BMC for normal operation. Fig. 6-2 illustrates the functions involved and is keyed with circled numbers to a summary of the Data Transfer Sequence. The transfer operation is described here in phases of Request Initiation, Servicing, and Termination. Prior to these phase descriptions is a description, BMC setup, defining operations necessary at system initialization or sometime prior to the transfer operations.

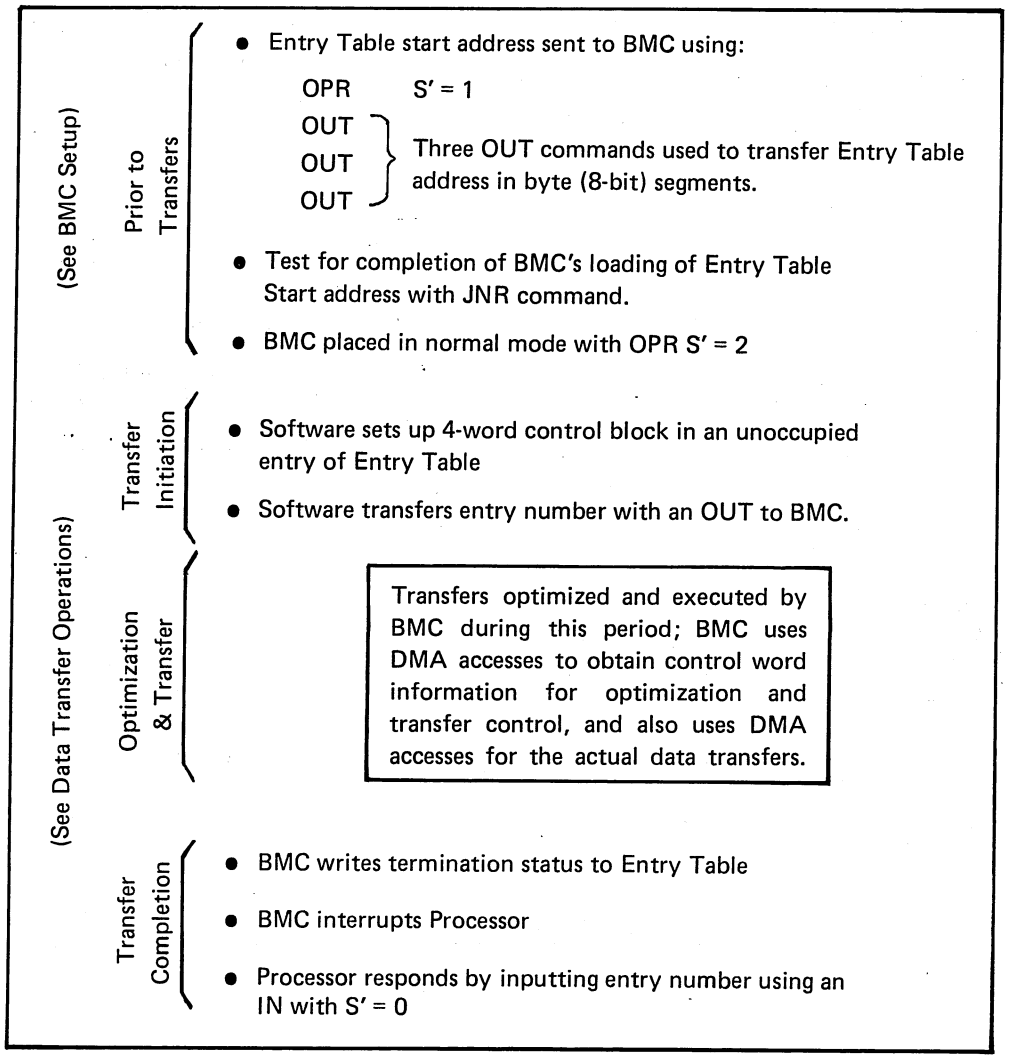


Table 6-2 Data Transfer Operations

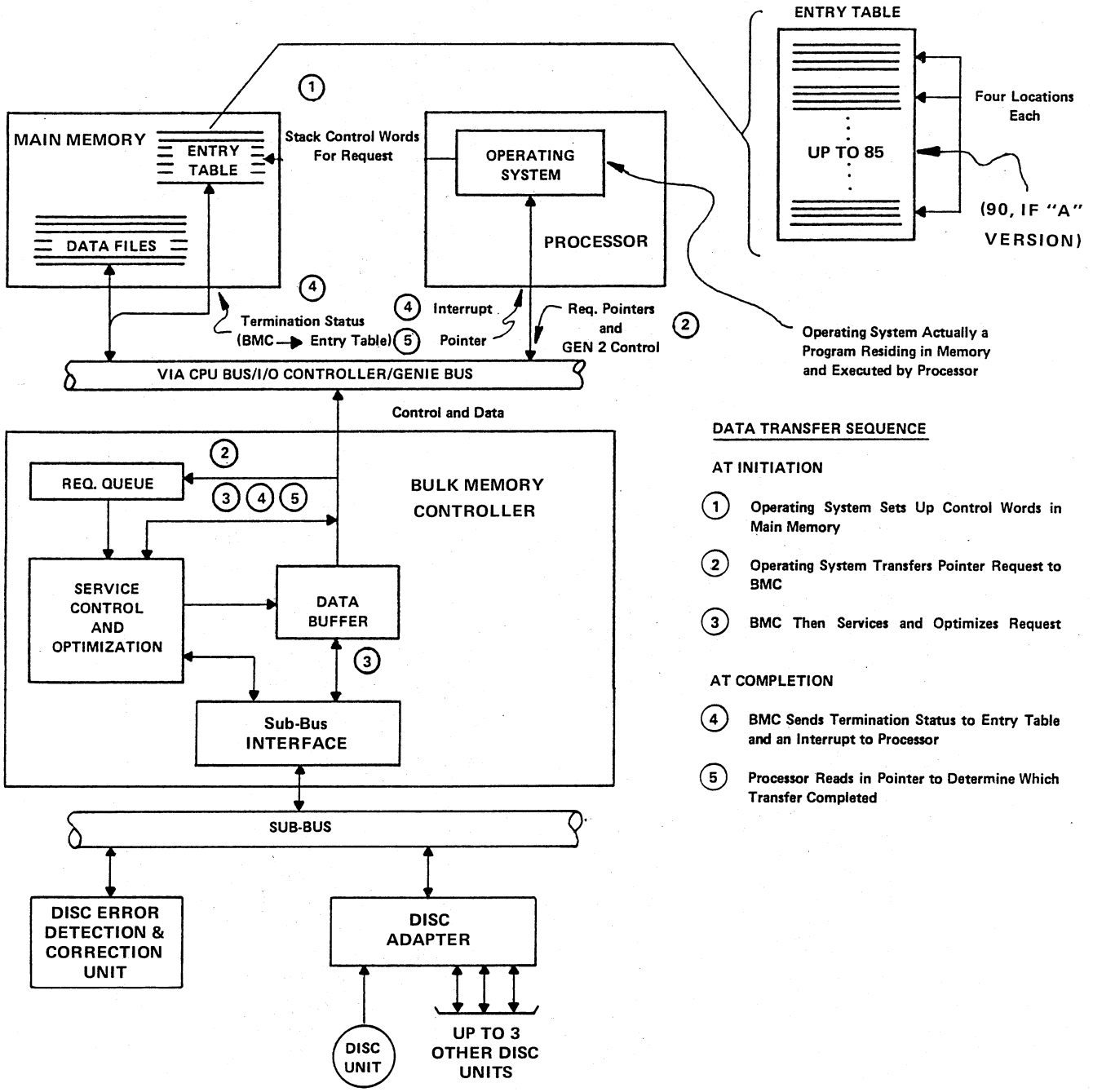


Fig. 6-2 Functional Block Diagram - MHD Subsystem

6.4.2.1 Data Transfer Request Initiation

Prior to transmitting an actual transfer request to the BMC, the operating system must set up a four-word control block, defining the transfer, in the Entry Table. As indicated in Fig. 6-2, the table can hold up to 85_{10} (90_{10}, if "A" version) four-word entries. The format to be used is shown in the right hand column of this page.

There is no priority related to the order of the control word listings. Requests are normally serviced in an order determined by the BMC optimization routine. Each control word block loaded in the table is keyed by an entry number sent to the BMC. All further accesses to the control word block from the BMC are keyed by number - to obtain address information for optimization and for transfers, and finally, to transfer the termination status.

Pointer requests are sent to the BMC using an OUT command addressed to the controller. The 8-bit information item from the A Register during the command's execution defines the entry number, where 00 is the first entry, 01 is the second, and 84_{10} (89_{10}, if "A" version) the last. An example of a pointer request and the ultimate accesss address is shown in Table 6-1.

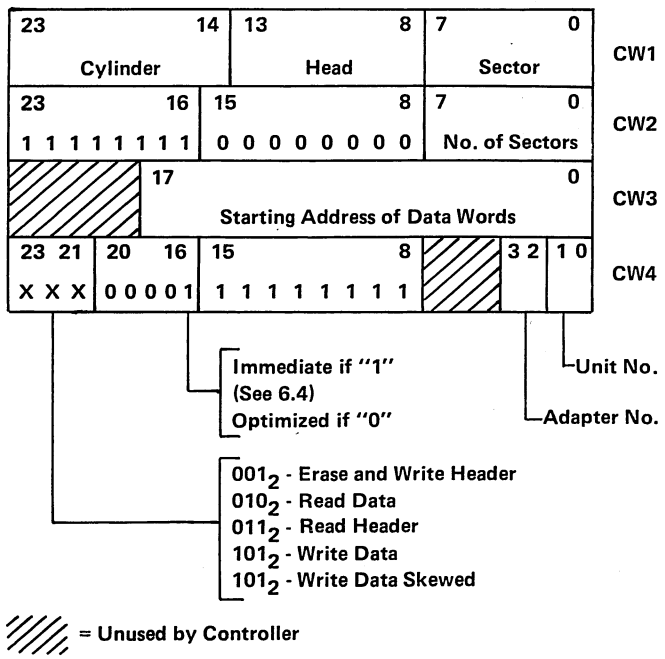
6.4.2.2 BMC Service of Transfer Request

Each entry number sent to the BMC represents a transfer request. As they are received, they enter a 64-entry queue from which they are processed whenever the BMC completes a request. Since requests can be stacked at a much faster rate than transfers can be performed, these requests are examined by the BMC between transfer operations to determine the desired disc addresses. This information is used for optimization of head movements and for scheduling transfers in rotational order. (See Primary Features.) Optimization information for up to 85_{10} (90_{10}, if "A" version) Entry Table entries can be stored in the BMC's memory.

When an actual transfer is initiated, the BMC uses DMA accesses to obtain the control words for the transfer. Following the transfer, the BMC performs the transfer completion phase.

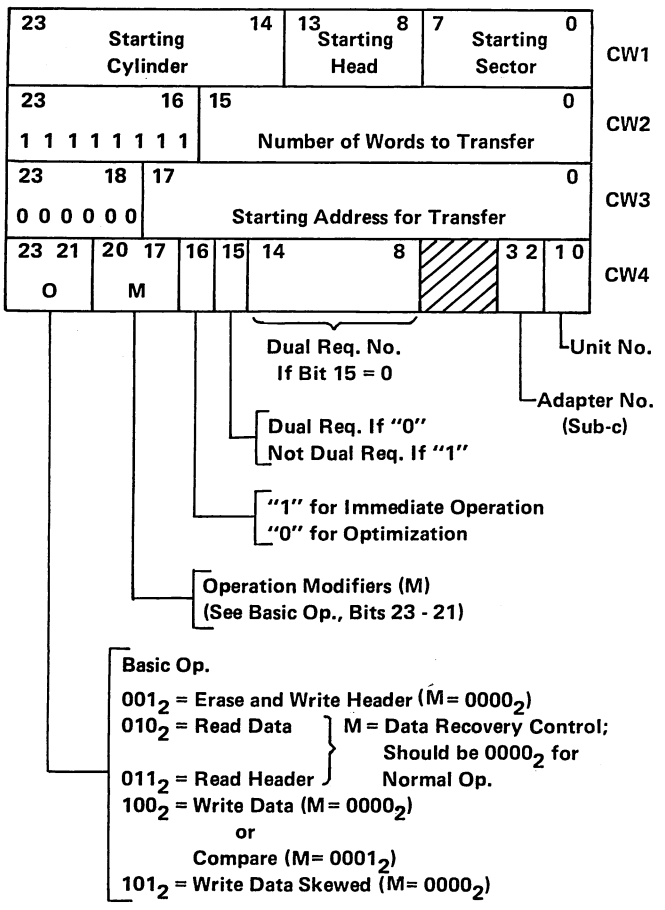
Control Word Formats for Data Transfers

"A" VERSION (SEE "OPTIONS", 6.2)



= Unused by Controller

"B" VERSION (SEE "OPTIONS", 6.2)



= Unused by Controller

Read Data Operation

Data is read from the specified cylinder, head, and sector into memory starting at the address specified in CW3. From 0 to 65535 (255, if "A" version) sectors of data may be transferred with a single command. If a request crosses heads or cylinders, the BMC will perform any head changes or head movements.

The transfer operations (Read Data, Write Data, Write Data Skewed, Write Header, Read Header, and Compare Data, if "B" version) may use an immediate flag to specify that the request is to be processed as it is recognized rather than being held for optimization. (Refer to the Entry Table control word formats for immediate codes versus optimizing codes for the operations mentioned.)

Notes on Read Data Completion

Upon termination, the address of the last cylinder, head, and sector read (not the next address) is stored in CW1. If the transfer terminated abnormally, the number of sectors remaining to be transferred is stored in bits 15 - 0 of CW2, otherwise bits 15 - 0 are zeroed. (For "A" versions, bits 7 through 0 of CW2 contain the number of sectors successfully transferred.) Certain DMA or uncorrectable ECC errors can cause the sector following the last sector successfully transferred to be undefined.

If a fatal 506 or 510 error (Header parity or Address Comparison, see 6.4.6) occurs, the controller transfers the data following the unreadable header, showing the transferred sector in the termination transfer count. This data may or may not be the correct data for the unreadable header.

Compare Data Operation ("B" Version Only)

Data is read from the specified cylinder, head, and sector and is compared with the data from memory which starts at the address specified in CW3. From 0 to 65535_{10} sectors of data may be compared with a single command. If the request crosses heads or cylinders, the controller performs the crossover. Termination status and control words are updated as for Read Data. If the comparison fails on any sector, a Comparison Error will be returned with the transfer count showing the number of sectors unsuccessfully compared and CW1 specifying the sector which failed the comparison.

Write Data Operation

Data is written on the specified cylinder, head, and sector starting with the CPU memory address specified in CW3. From 65535_{10} (255 if "A" version) sectors of data may be transferred with a single command. If the request crosses heads or cylinders, the controller performs the crossover.

Notes on Write Data Completion

If any sector is encountered with a sector write protect bit set in the header (most significant bit of first word of header, if "A" version; least significant bit of first word of header, if "B" version) or if the Unit Write protect is enabled, a 440 error (see 6.4.6) is immediately returned with the transfer count showing the number of sectors written and CW1 specifying the sector having the write protect.

Write Data Skewed

Externally identical to Write Data. The data written on the unit consists of seven leading zeros. The last seven bytes of the data from the CPU are written as the Error Correction Code bits of the sector.

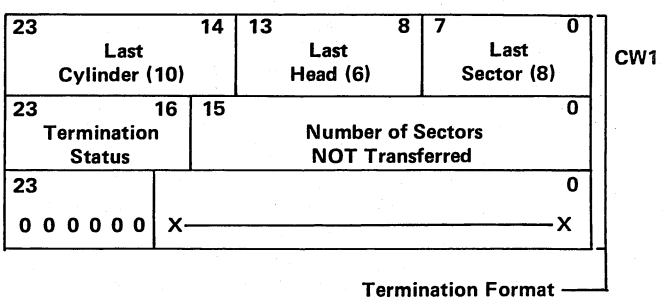
This operation is used only to test the operation of the error correction hardware.

6.4.2.3 Transfer Completion

A transfer completion for a Read Data, Write Data, Write Data Skewed, or Compare ("B" version only) operation is indicated by an interrupt from the BMC. The completion may have been a successful transfer, a transfer with a corrected error, or an incompleted transfer with an uncorrectable error. This is indicated by the coded information placed in the entry table prior to the interrupt. (Refer to 6.4.5 for the format of the codes placed in the control words upon transfer completion.)

The control word status following completion will appear in the following format:

Read Data/ Write Data/Write Data Skewed/
Read Headers/Erase and Write Headers
Completion Status



6.4.3 Header Transfer Operations

Header transfer operations are used to establish and recover the control information (other than data) for each sector. Fig. 6-3 shows the area recorded by an Erase and Write Header operation. A Read Header operation can then be performed to verify the information. A subsequent Write Data operation is required to provide the data and correct checksum for each sector. Initiation, servicing, and completion of header transfer operations, are similar to that of data transfer operations (6.4.2).

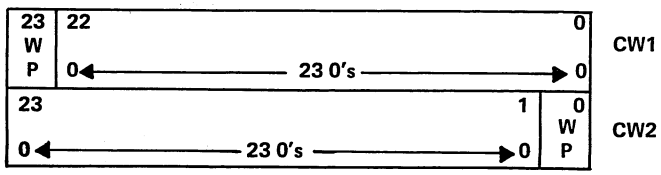
Erase and Write Header operations write one 64-sector track of header information per request. A Read Header operation reads the two-word sector headers in a manner similar to Read Data. From 0 to 65535_{10} (255 if "A" version) sector headers may be read. The sequence of these operations is essentially the same as Write Data and Read Data operations. The uniqueness of their operation is defined by the Initiation Status provided in Control Word 4 of the Entry Table and the use of a Write Header switch in the BMC.

Erase and Write Header Operation

The Erase and Write Header operation uses the specified head and cylinder information of Control Word 1 to begin writing header information as supplied from the memory area starting with the address specified in Control Word 3. Sixty-four headers are written on the track using information from 128 data words.. The Erase and Write Header operation must be followed by 64 sectors of Write Data operations to establish a correct data checksum for each of the 64 sectors.

To set the sector write protect feature (6.3.4), bit 23 of the first data word and bit 0 of the second data word should be set. The remaining 46 bits should be zero.

Termination status for a Write Header operation is as follows:



WP = Sector Write Protect

Termination status is the same as for Write Data (6.4.2.3). Error codes are defined by 6.4.6. Typical uncorrected error codes may be 440 - Write Header switch not enabled or 544 - unit Write Protect switch set.

Read Header Operation

The Read Header operation reads data from the 2-word header area of each sector starting at the specified cylinder, head, and sector. Each sector transfers two words of data to memory starting at the address specified in CW3. Termination status and control words are updated as for Read Data operations (6.4.2.3).

6.4.4 Control and Test Operations

There are three operations described here under the category of control and test. One is considered as test (Read Characteristics) and two are regarded as control (Cancel and Reset).

Read Characteristics acts as a "snapshot" status check for disc units.

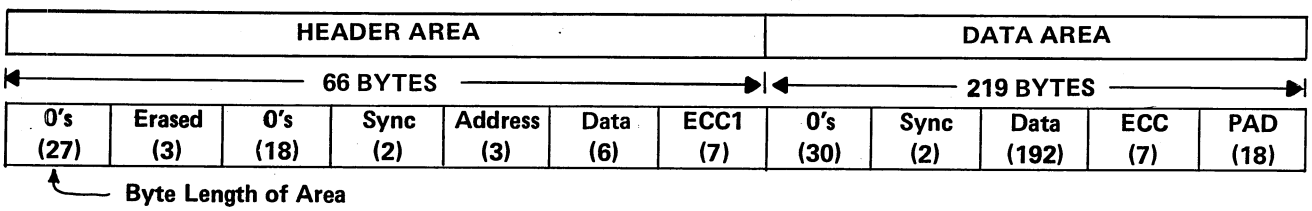


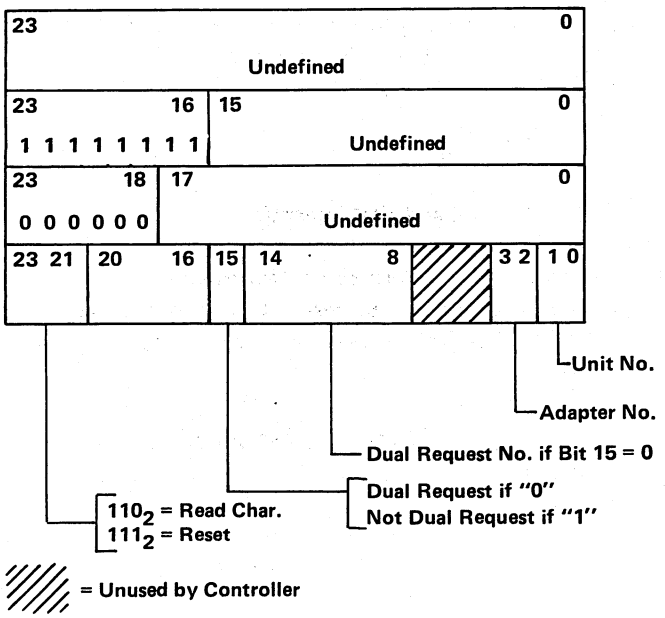
Fig. 6-3 Sector Format

Cancel permits the termination of a queued transfer request before its completion. Reset initiates a return-to-zero head movement on the specified disc, resets any errors related to the unit and then performs a Read Characteristics operation.

The control word formats for entry and termination for each of these operations is described by the following text. The operational sequence is the same as described for data transfer operations, with a setting up of control words and then the request initiation via an Entry Table entry followed by the actual operation and the request termination.

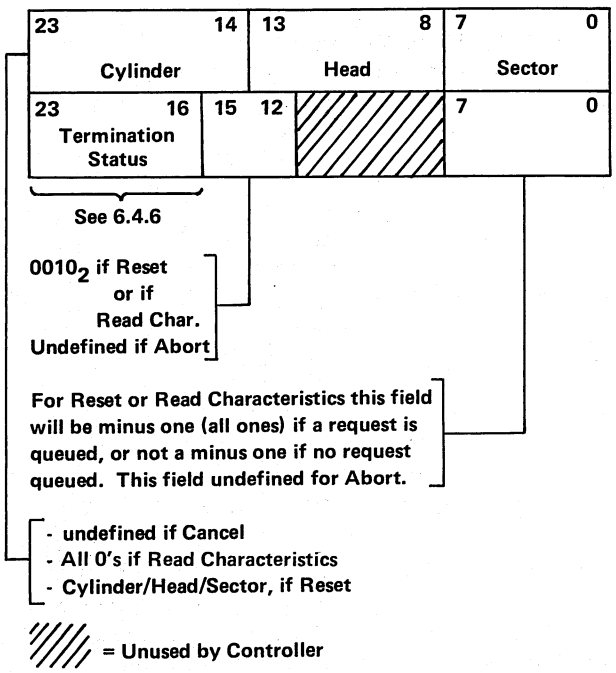
READ/CHARACTERISTICS/RESET

Initiation Status (for either "A" or "B" version)

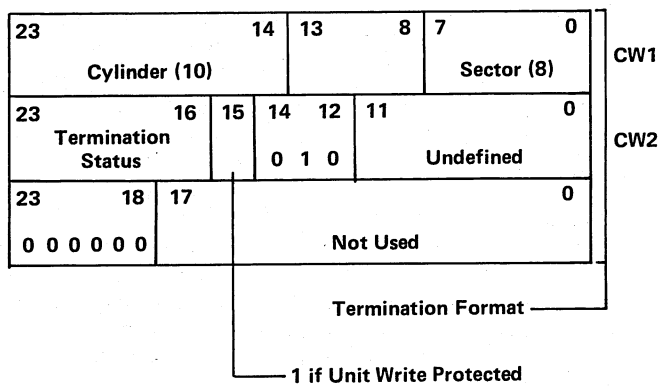


There are two formats for termination status, as indicated by the following formats:

TERMINATION STATUS FOR "A" VERSION



TERMINATION STATUS FOR "B" VERSION



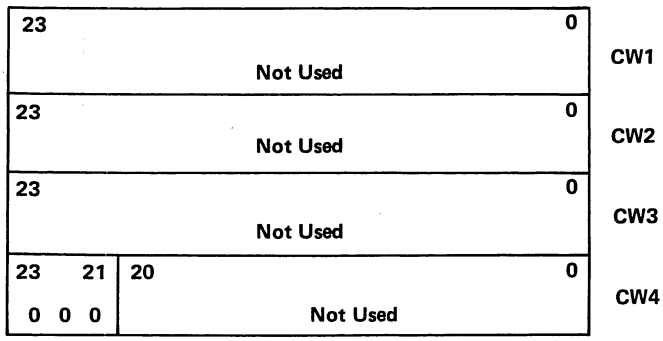
Read Characteristics

Upon detecting the OUT the controller immediately returns the current unit status and BMC characteristic code 010. CW1 contains the current unit cylinder.

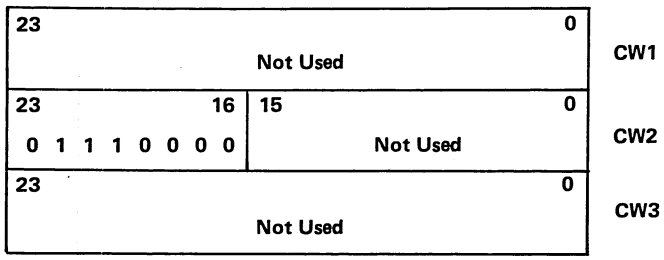
A fatal termination status means only that the unit would not be ready to accept a command at this time. The Read Characteristics operation will always complete if the BMC is operational.

Cancel

Initiation Status



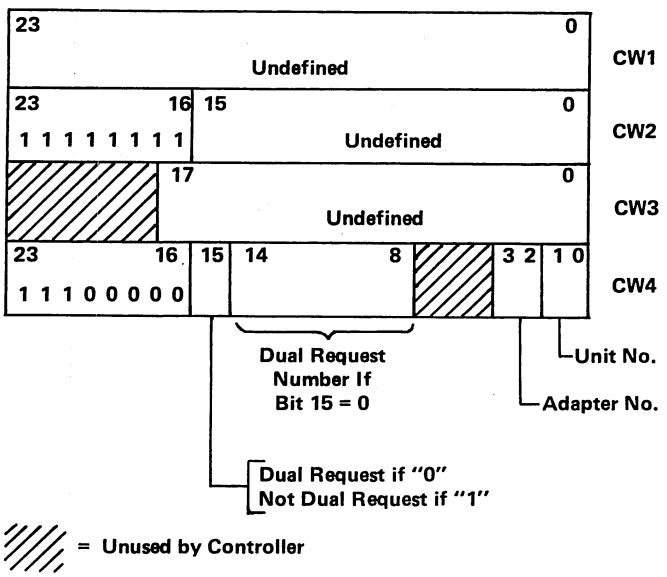
Termination Status



Upon detecting the OUT the controller immediately returns the entry with the status marked CANCEL ACKNOWLEDGE. This command can be used to clear an entry that had been previously issued to the controller with another operation code. Only the termination status is altered by this request.

RESET

Initiation Status



Termination Status

(See Read Characteristics/Reset Termination Status.)

Operation

Upon decoding the OUT the controller issues an RTZ (Return-To-Zero) and reset errors command to the unit and then performs the operations of Read Characteristics.

Unique Status

The status returned is that following the RTZ, which would normally be 572, off cylinder. If the unit has hardware problems or is off-line, another status will be returned.

6.4.5 Termination Codes

The following is a definition of termination codes other than errors. The code value shown is the octal value of bits 23 - 16 of CW2. Error termination codes are specified under 6.4.6.

Code	Significance	Source
000	Normal Termination	BMC
340	Abort Acknowledge	BMC
772	Late Start - Dual Request was Initiated First	BMC
774	Requested Data Transfer Initiated and In Progress	BMC
776	Initial Status	CPU Request Routine

6.4.6 Alarms/Error Detections

There are several levels of error checking used in the Moving Head Disc Subsystem. Data and control functions are checked at each level of operation and reported for software and/or operator response. Basically, there are three methods of reporting detected errors:

1. I/O Bus Alarm
2. In Pointer Bit 7
3. Termination Status

An I/O Bus alarm occurs if any device controller on the bus transmits incorrect parity on an arbitration cycle (for either memory request or interrupt request) or if any device controller fails to respond to a transmission from the Bus Controller (i.e., Timeout error). The error is indicated by the I/O Bus alarm light and is program detectable by a JNE command addressed to the I/O Controller.

Bit 7 of the pointer byte read by an IN command addressed to the BMC, when set, indicates a DMA error occurred during access to the control word of the completed transfer.

A number of errors can be reported in the termination status. The termination status is a code placed in a specified area of the information supplied to the Entry Table for the completed transfer. These codes (which are represented as left-justified octal numbers with bit 15 not used) represent errors detected at the disc unit, subcontroller, and Bulk Memory Controller levels. They are defined as follows:

Disc Unit Detected Errors

Code	Error Definition
540	Unit Write Protected
542	Seek Error - Invalid Cylinder Address
544	Head Select Fault
546	Voltage Fault in Unit
550	Write and Read Selected Simultaneously
552	Write or Read with Off-Cylinder Fault
554	Write Fault (Fault while writing)
556	Invalid Head Selected
562	Offset Active Fault
570	Unit Not Ready
572	Unit Off Cylinder

Disc Adapter Detected Errors

Code	Error Definition
600	Loss of Servo Clock
602	Multiple or No Unit Select Error
604	Controller/Adapter Interface Timing Error
606	Adapter - Unit Timeout

Bulk Memory Controller Detected Errors

Code	Error Definition
042	Correctable EDAC Error(s) with No Retry
044	EDAC Error Corrected on Retry after Initial Uncorrectable Attempt
440	Sector Write Protected
442	Correctable EDAC Error(s) with Other Fatal Errors
444	Uncorrectable EDAC Error(s)
446	Comparison Error - Data Error on Compare Operation
502	No Address Mark
504	No Header
506	Header Parity Error
510	Address Comparison Error
512	No Data Following Header
610	Parity Error within EDAC Unit
620	Unit Address Readback Error
622	Adapter Select Error
624	No Unit
642	Overrun (read) Underrun (write)
702 ↓ 736	DMA Interface Errors

6.4.7 Command Descriptions

Table 6-3 provides a summary listing of the GEN 2 commands used for BMC control. Each command is described here in the order listed, under headings shown in the Function Type column.

ACT, S' = 0, sets the BMC's inhibitable interrupt as if there had been a transfer completion, but does not specify the data read by a subsequent IN command.

AIM, S' - 6, activates the interrupt inhibit mask, blocking generation of interrupts.

DIM, S' = 7, deactivates the interrupt inhibit mask, permitting generation of interrupts.

OPR commands should only be issued when the channel shows a non-busy status. An ABT command can be issued to force the channel to this status as checked by JNR.

OPR, S' = 0, produces a program load sequence. Upon receipt of this command, the BMC enters a channel-busy condition where it initiates a read of 1 sector of data from adapter 0, unit 0, cylinder, head and sector 0 starting at location 0 in memory. If the transfer completes successfully, the BMC returns to a channel non-busy status. If it does not complete successfully, the BMC continues to retry the operation and remains in a busy status unless an Abort is issued or a System Reset occurs. No memory locations other than 0 through 77_8 are affected by this operation.

OPR, S' = 1, sets the BMC in the Load Entry Table Address mode. Upon receipt of this command the BMC enters a channel busy condition. The Entry Table is then loaded by three OUT commands (see OUT S' = 1), each of which transmits an 8-bit byte of data. Address bits 0 through 7 are sent with the first OUT command, followed by bits 8 through 15 on the second. (Each transfer transmits the data on bus data lines 0 through 7.) The third OUT transmits bits 16 and 17 of the address on bus data lines 0 and 1, respectively. Bits 3 through 7 of the third transfer are not significant for either the "A" or "B" versions. The "B" version, however, does examine bit 2 of the third transfer to determine the compatibility mode. If bit 2 of this transfer is reset (logic 0), the BMC functions in a compatible manner with the "A" version BMC operation. This means that the newer "B" version BMC functions would not be operational, such as the breakoff mode, mag tape or ISL operation. After the third OUT is processed, the BMC returns to a channel not-busy state.

OPR, S' = 2, sets the BMC in the Normal mode to accept point word requests, as described in 6.4.2.

OPR, S' = 3, sets the BMC in the Loopback mode causing a return of data sent on subsequent OUT commands while still in the same mode. The information is gated back to the Processor's A Register by execution of an IN command. If interrupts are permitted, an interrupt will be set following the OUT command, indicating that the data is ready for input. (Used for testing Processor/BMC interface.)

OPR, S' = 4, sets the BMC in the Idle mode. This causes the BMC to initialize itself, ignoring subsequent requests until receipt of another OPR command to switch to another mode. The BMC is automatically set in this mode by a System Reset or an unconditional abort.

ABT, S' = 0, provides a Port Abort (designated "Conditional Abort" on "A" version) to initiate an orderly termination of all BMC operation currently in progress, thereby freeing the BMC for an alternate subsequent action. Upon receipt of this command, the BMC remains in a channel-busy state until any request in progress can be stopped. All current requests are then aborted, and the BMC goes not busy. BMC action is terminated at the earliest time that permits orderly shutdown, preserving the integrity of all monitoring functions and any data movements currently in progress.

This abort terminates operations as soon as the data transfer, if any is completed. Termination awaits completion of the current sector. In either case, the only affected indicator, channel busy, is set not busy at the time BMC action ceases.

ABT, S' = 1, causes an immediate, unconditional initialization of the "A" version BMC and of the "B" version BMC, if so selected by a pinning option of the "B" version's Port PWA. (Otherwise it functions as a Port Abort on the "B" version BMC.) Since all BMC actions are cleared by this command, it is the responsiblity of the user to regain memory unit synchronization and to recover any data destruction that might have occurred.

OUT, (Modes "Load Entry Table Address"; see OPR, S' = 1) transfers the Entry Table starting address to the BMC. It also transfers (see OPR S' = 1) the compatibility mode for the "B" version BMC. The BMC must have been previously set to the OPR mode to correctly interpret the starting address and compatibility data. Three OUT transfers must be executed to transfer the entire address, using the following conventions:

1. OUT # 1 Bits 0 - 7 of A Register represent bits 0 - 7 of Entry Table starting address

2. OUT # 2 Bits 0 - 7 of A Register represent bits 8 - 15 of starting address

3. OUT # 3 Bits 0 and 1 represent bits 16 and 17, respectively, of starting address; bit 2 represents compatibility mode, if "B" version.

These transfers are required only at system initialize to establish the starting Memory address of the Entry Table, which vary from system to system.

OUT, (Mode = "Normal"; see OPR, S' = 2) transfers the entry number in bits 7 - 0 of the A Register to the BMC. This entry number is stacked in and serviced from a FIFO Register in the BMC.

OUT, (Mode = "Loopback"; see OPR, S' = 3) transfers data to the BMC for readback in Loopback mode. (The BMC must be set to the OPR, S' = 3 mode for correct usage of this information.)

IN, S' = 0, transfers eight bits of information from the BMC to bits 0 - 7 of the Processor's A Register. Significance of the data is determined by the mode set by a previous OPR command. Bit 23 is used to indicate whether an interrupt is present. If an interrupt was present, indicated by bit 23 = 0, the data is valid; if an interrupt was not present, bit 23 = 1, the data is considered invalid. Bits 8 through 22 are set to zeros during an IN command.

IN, S' - 1 operation and data transfer is identical to IN S' = 0 except that the data output latch of the controller is not cleared. This instruction is useful in polling the controller to see if data is present when operating the controller without interrupts. The following code should be used to take data from the controller without interrupts:

```
LDX -Controller Address-, 3
IN /10,3      Get interrupt and data status
TOD 23        Valid data present?
BTS *-2       No. Try again.
IN  0,3       Yes. Get the valid data.
.
.
.
```

JDR, S' = 4 senses the status of the BMC ready line. It will appear not ready, causing a P counter jump of relative plus two, if the 64-position input queue of the BMC is full. If a not ready indication is received, an OUT command should not be issued to the BMC.

JNR, S' = 0 senses the status of the BMC busy line, causing a P counter jump to relative plus two if the BMC is busy (not ready). The BMC is set busy by the following:

1. Receipt of ABT. (Busy resets when all requests are aborted.)

2. Receipt of an OPR. (Busy resets after modes S' = 0 or S' = 1 complete.)

JNE, S' = x (x = insignificant) senses the presence of any alarm conditions detected by the BMC at the time of this command's execution. It can be executed at any time without affecting BMC action. An alarm indication, causing a P count increment of one, indicates an error in the BMC's interface with the GENIE Bus. Errors in disc units or subcontrollers are reported in the termination status sent to the Entry Table upon completion of a transfer.

6.4.8 BMC Interrupts

The BMC uses an inhibitable interrupt line to indicate transfer completion. Transfer completion occurs when the BMC has fully serviced a request placed in the Entry Table. The interrupt line can also be triggered by execution of an ACT, S' = 0 command.

6.5 ADDITIONAL CHARACTERISTICS

6.5.1 Disc Unit Primary Power

See 3.2.4 in Section 3.

6.5.2 Disc Unit Physical Characteristics

The units are approximately 36" high, 36" deep, and 22" wide. The approximate weight is 345 lbs. and the units are caster mounted for mobility. Leveling pads can be lowered to raise disc units off casters once in position.

6.5.3 Environmental Classes

The units are class C (see 3.1 and Table 3-1). The BMC and adapters are housed in the CSU and are class A.

MNEMONIC	S	S'	FUNCTION PERFORMED	FUNCTION TYPE
ACT	1	0	Set Transfer Complete Interrupt	INTERRUPT CONTROL
AIM	1	6	Activate Interrupt Inhibit Mask	
DIM	1	7	Deactivate Interrupt Inhibit Mask	
OPR	2	0	Set "Program Load" Mode	BMC MODE SELECTION
OPR	2	1	Set "Load Entry Table Address" Mode	
OPR	2	2	Set "Normal" Mode	
OPR	2	3	Set "Loopback" Mode	
OPR	2	4	Set "Idle" Mode	
ABT	3	0	Port Abort (Conditional Abort, if "A" version)	ABORTS
ABT	3	1	Unconditional Abort ("A" version only)	
OUT	4	–	Output Entry Table Address (Note 1)	INFORMATION TRANSFERS
OUT	4	–	Output Entry Number (Note 2)	
OUT	4	–	Output Loopback Data (Note 3)	
IN	5	0	Input Loopback Data or Entry Number and Acknowledge Interrupt	
IN	5	1	Check Availability of Input Data (S'=0)	
JDR	6	4	Jump if BMC FIFO Not Full	TESTS
JNR	6	0	Jump if Not Ready (See Text)	
JNE	7	–	Jump if No Error (See Text)	

NOTES

1. If previously set to "Load Entry Table Address" mode by OPR S' = 1.
2. If previously set to "Normal" mode by OPR S' = 2.
3. If previously set to "Loopback" mode by OPR S' = 3.

Table 6-3 GEN 2 Command Summary

MODULAR FURNITURE

Members of the Modular Furniture family are combined to form Process Operator/Engineer complexes that are attractive, functional, and comfortable. The basic building block for the Modular Furniture complexes is a 29-inch high table, which is available in widths of approximately 24", 46", 68", or 91" (one, two, three, or four lower compartments) and depths of 48". The table options include cable ways and mounting kits which accommodate the power cables and interconnecting cables to the devices installed in or on the tables, ac distribution centers with circuit breakers and outlets, paper trays, and pencil drawers. Corner wedge frames and tops are available to form shaped table complexes. Video Display enclosures are available which accept one, two, three, or four 15" monochromatic Display Monitors or 19" Color Display Monitors (Sections 9 and 10). Fig. 7-1 illustrates the appearance of a typical Modular Furniture configuration with Video Display Monitors and keyboards built into the console. Fig. 7-2 provides top/side views of a combination of Modular Furniture items forming an Operator/Engineer complex.

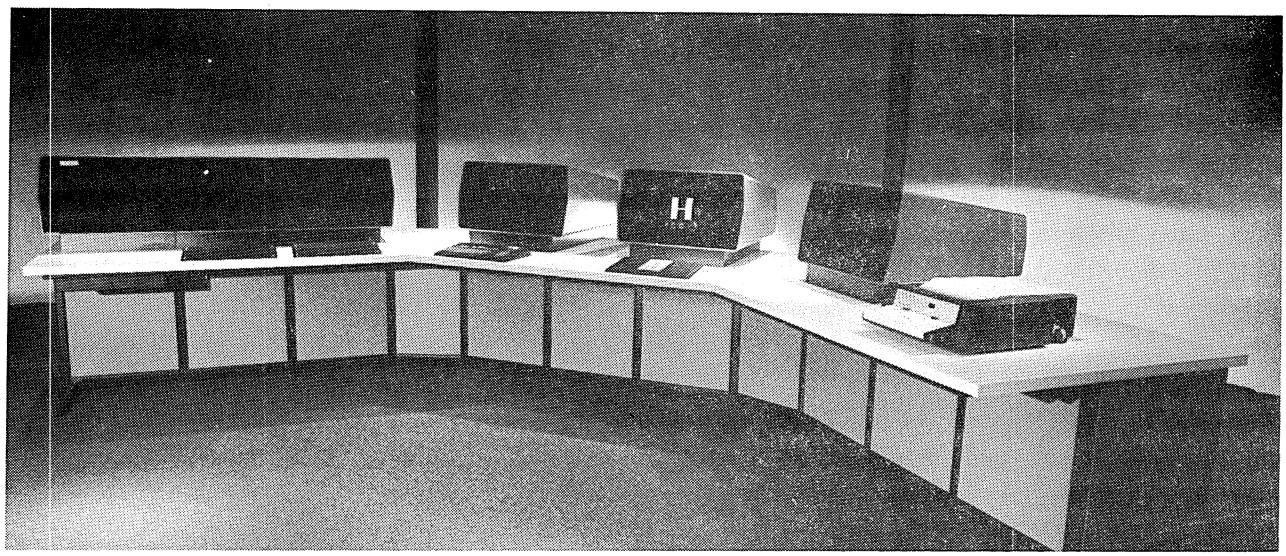


Fig. 7-1 Modular Furniture Combinations With Video Displays

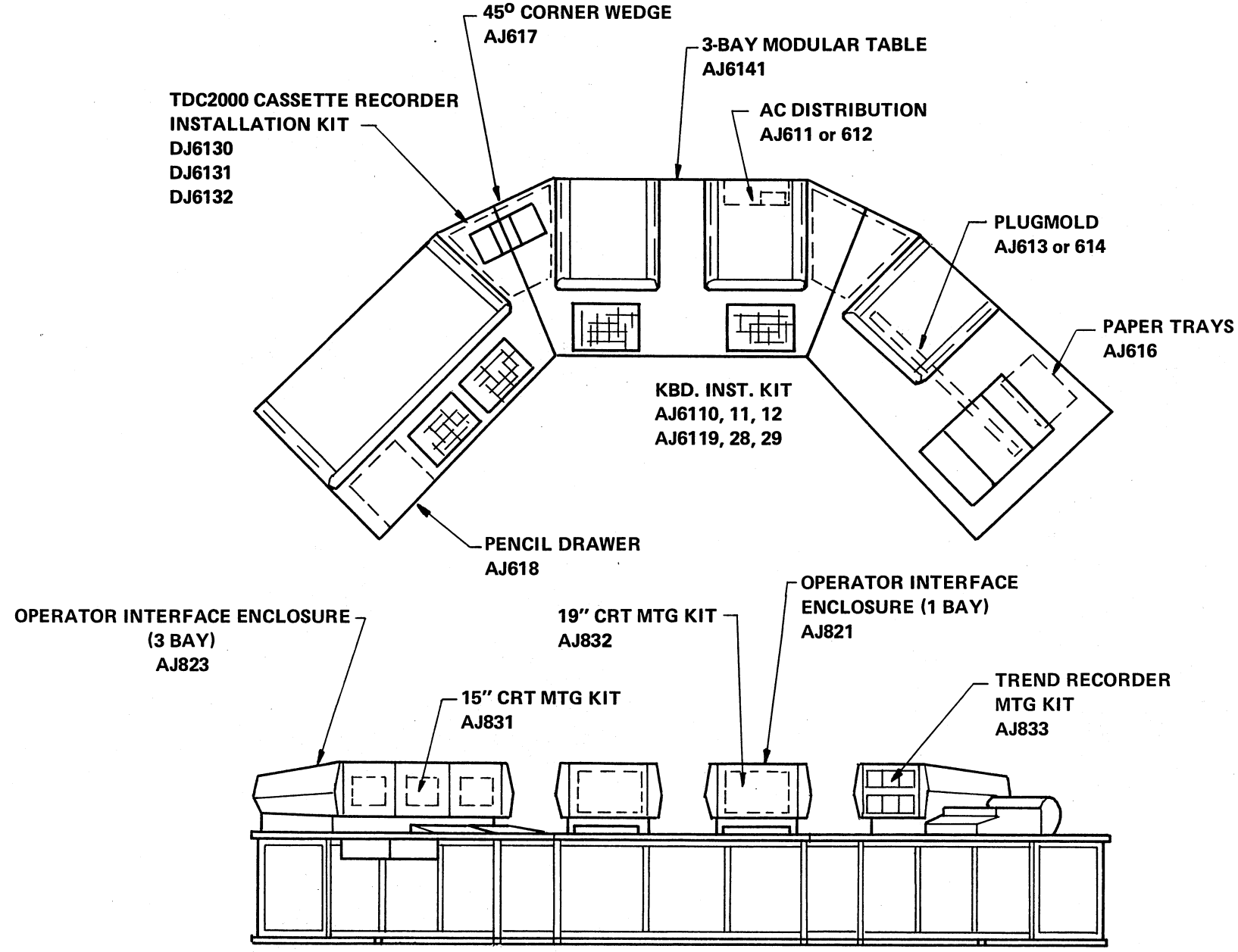


Fig. 7-2 Typical Console With Most Options Shown

PERIPHERAL DEVICES

The peripheral device subsystems described in this section are those used by operators, programmers, technicians, and engineers for the entry and retrieval of computer information. Other devices, such as Drum and Disc Memories, Process Operator Consoles, and Video Displays may be considered to be peripheral devices, but are not included in this category, and are described in other sections of this General Description.

The devices included in the Peripheral Device category include typers, paper tape readers and punches, card readers and punches, and line printers. All are freestanding devices, and all but the card punch and line printer may be table mounted. The Modular Furniture described in Section 7 of this manual provides ideal facilities for table-mounted devices.

Every TDC 4500 system must have, as a minimum peripheral device complement, at least one input/output typer for communication with running programs and one card or paper tape reader for program loading.

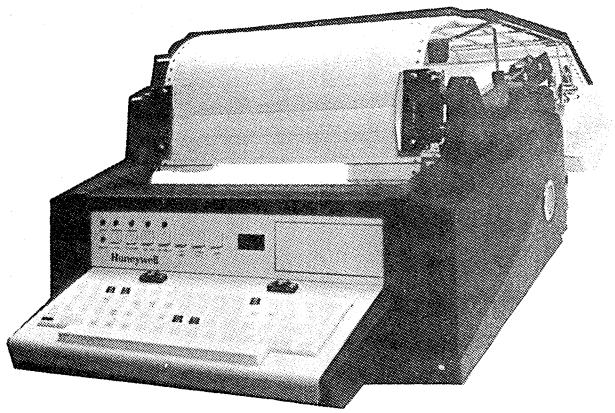
All of these peripheral devices interface with the Central Processor via controllers on the GENIE I/O Bus (4.5). The device operations may be divided into two basic classes - input operations and output operations. For input operations, data are sensed from cards, tapes, or keyboards for transfer through the Arithmetic Unit to main memory through the use of GEN 2 instructions or the TIM feature. For output operations, data are transferred from main memory via the Arithmetic Unit, through the use of the TOM feature or GEN 2 instructions, to be recorded on cards or paper tape, or to prepare a printed record. The data are transferred in characters consisting of 7 or 8 bits or halfwords consisting of 12 bits. The data are transferred to or from the least significant bits of the A Register when transferred by GEN 2 instructions IN or OUT.

Input and output messages are formed by combining several characters into an appropriate message format. Message control characters which affect the devices or their controllers on the GENIE Bus are indicated in the device descriptions which follow. All peripheral devices may be operated at their full rated speeds while other peripherals and subsystems are operating.

8.1 PRIMARY POWER

Each of the peripheral devices is furnished with a power cable and plug. The primary power is supplied by the customer in the form of standard three-pin wall outlets (two wires plus safety ground). 115 Vac ±10% at 60 Hz ±1% (50 Hz ±1% optional) is normally required.

8.2 TermiNet PRINTERS



TermiNet Printers are quiet, compact units, in which most functions are accomplished electronically, minimizing mechanical functions. Printing is accomplished by a rotating-type belt that contains two character sets, and prints the characters by firing a hammer as the correct character passes the desired position on the print line. The TermiNet 300 Printer communicates with the computer and prints at 30 characters per second while the TermiNet 1200 Printer operates at 120 characters per second.

Both the TermiNet 300 and TermiNet 1200 Printers are available as receive only (RO) devices and as keyboard send and receive devices (KSR). The following basic TermiNet Printer models are available:

ASPA2 TermiNet 300 KSR

ASPB2 TermiNet 1200 KSR

ASPA1 TermiNet 300 RO

ASPB1 TermiNet 1200 RO

8.2.1 TermiNet Printer Options

The following descriptions apply equally to the TermiNet 300 and TermiNet 1200 Printers except where specific references to one printer or the other are made.

Print Line Length and Paper Feed

The printers are available with print lines of 118 characters. The first I/O typer implemented in a system normally serves as the programming and maintenance I/O typer. All units include an external paper handler.

In TermiNet 300 Printers, the 118-column version features a pin-feed platen that accommodates paper 12-27/32 inches in width, with a horizontal separation between feed pin holes of 12-11/32 inches.

In TermiNet 1200 Printers, the 118-column version features pin-feed tractors that can be adjusted to accept any paper width, but are normally used with paper 12-27/32 inches wide with 12-11/32 inches pin-to-pin spacing. The 118-column printer actually can print 120 characters on each line, but the final two characters are printed at the right edge of the paper where multi-part paper has a tear strip.

Vertical Tab and Form Feed Option*

This option is virtually mandatory when fan-folded paper is used. It is designed for paper with an 11-inch form length (66 lines per page). The top-of-form position and the vertical tab positions are specified by holes punched in a special tape by the user. A vertical tab code (VT, 013_8) transferred from the computer or generated at the keyboard slews the paper to the next vertical tap position. A form feed code (FF, 014_8) transferred from the computer or generated at the keyboard slews the paper to the top of the next form (page).

Horizontal Tab Option

When this option is present, the horizontal tab positions may be set at the current character position at the keyboard or through the computer transferring ESC (033_8) and 1 (061_8). A horizontal tab code (HT, 011_8) generated at the keyboard, or transferred from the computer, moves the current character position to the next tab position. All tabs are cleared on loss of power.

Parity Error Detection Option

The TermiNet Printer hardware generates an even parity bit to accompany each character transmitted to the computer, and the I/O controller on the GENIE Bus generates an even parity bit for each character transferred to the printer. The parity detection option for the printer prints a diamond, generates an audible alarm, and lights the interrupt light on the printer when a character is received from the computer with incorrect parity but no indication is returned to the computer. This option is useful when the TermiNet is located remotely from the computer and the two sites are interconnected via data sets and telephone lines.

Computer Interface

Where the computer and the printer can be connected by up to 50 feet of cable, a voltage interface is used for a direct connection to the printer. Where the computer and the printer sites are separated by a considerable distance, a modem interface is used, with a data set at the computer site, and a built-in modem (data set) in the printer. In both cases, the printer and computer interfaces comply with EIA standard RS-232C. These interfaces provide a printer status line to the computer (the EIA Data Terminal Ready line) that indicates a printer alarm condition when the printer detects low paper, shield up, low voltage, or low tape.

A direct connection with up to 2000 feet of cable may be made when the current loop interface option is used. This interface returns alarm status to the computer as is returned over the voltage or modem interface. This interface also returns a continuous break signal on the input line to the computer when the printer is in Local Mode, has ac power off, or is not connected to the computer. This continuous break condition may be detected by JNE S' = 0 addressed to the input channel (see Alarms under 8.2.4).

Both interfaces return a momentary break to the computer when a printer alarm occurs or when the Interrupt button on the printer is pushed. The momentary break sets the alarm flip-flop in the controller and the alarm line may be tested by JNE S' = 6 addressed to the input channel (see Alarms under 8.2.4).

Red/Black Printing

TermiNet 300 RO Printers may include this option. It causes the printer to print in red when the printer detects ESC (033_8) followed by 3 (063_8). As long as the ribbon is up for printing in red, the print line is obscured, therefore, ESC followed by 4 (064_8) should be sent to the printer after printing in red, to return to the print black mode, where the print line becomes visible when printing ceases. The red/black option is not yet available on TermiNet 300 KSR Printers.

*This option is not supported by the standard RTMOS software. The user must insert the proper codes and fill characters in his data string before making an output call to RTMOS.

Field Installation of Options

The following equipment options may be installed in the field by plugging in necessary modules: Integral model (300 baud or 1200 baud, as required by the printer), horizontal tab, parity error detection, and answerback (KSR units only). The remaining options must be implemented in the original printer order.

8.2.2 Operating Features

The printer prints all characters representing ASCII printable codes, including both upper and lower case letters. The keyboard is capable of generating all 128 ASCII codes, including all printable characters. The computer programs, however, typically recognize and transmit only upper case letters, so the All-Caps switch on the printer is normally set to the Caps position, to cause transmission of the upper case code when a letter key is pushed. Horizontal character spacing is 10 characters per inch, and vertical line spacing is either 6 lines per inch or 3 lines per inch, as selected by the Line Space switch on the printer. The printer is capable of printing up to a seven-part form (7 copies). A standard business-machine type ribbon is used which may be easily replaced per instructions affixed to the inside of the upper cover.

Since the printer is very quiet, an audible tone with adjustable volume is emitted as each key on the keyboard is pushed. A tone, which is higher in frequency than the key tone, and also has adjustable volume, is emitted when an alarm occurs and when a BEL code (007_8) is detected.

Character exchanges between the computer and the printer are bit-serial asynchronous, at 300 baud when the TermiNet 300 Printer is used, and at 1200 baud with the TermiNet 1200 Printer. A full duplex communications link is used, and when the printer is on line with the computer, it does not directly print characters transmitted to the computer, but prints the characters as they are "echoed" back to the printer from the I/O Buffer control in the computer. The printer recognizes characters from the computer, only, when on line, and responds to locally generated printing and control characters only when in the local mode. Each serial character exchanged between the computer and printer consists of a start bit, seven data bits, an even parity bit, and one stop bit, or a total of ten serial bits. The least significant data bit is moved first, and the data lines remain in the marking state in the absence of any data transmissions, so long as the printer remains on line.

For detailed descriptions of the operating controls, refer to maintenance publication no. 4172-6D-M, which includes the TermiNet Printer Operator's Manual and Programmer's Manual.

8.2.3 Message Formats

The descriptions which follow cover the basic message sequences and characters. The effect of the various control codes and necessary time fills that must follow some control characters are described in the TermiNet Printer Programmer's manual, which is included in maintenance publication no. 4272-6D-M.

Output to Printer

The program executes an Operate instruction addressed to the output controller on the GENIE Bus with 177_8 in the A Register. The output channel goes busy, the 177_8 character is not transferred to the printer, and the first data exchange interrupt occurs. The program then transfers the two motor-on characters (ESC, H)* and after sufficient fill characters or time delay for the motor to come up to speed, the program transfers the text characters. The final text character is followed by CR, LR, and sufficient fill characters, the motor-off characters (ESC, J)* are transferred, and the program then transfers DC4, which sets the channel not busy and generates the end-of-record interrupt.

*Control of the motor by the program is normally not necessary where an operator is present and he selects On-Line mode at the printer to turn the motor on when it is to be operated.

Keyboard Input

The operator pushes the Interrupt button on the printer which transmits a momentary break signal to the computer that makes the controller input channel go busy and then not busy, generating an end-of-record interrupt. The program then executes an Operate instruction addressed to the input channel with STX in the A Register. OPR sets the input channel busy and STX enables the echo-net function. As the operator strikes each key to transmit a character, the data exchange interrupt is generated when the complete character is held in the input holding register. The characters are input until the operator strikes the Return key which generates CR. When CR is input, the input channel goes not busy and the end-of-record interrupt is generated.

Baud Rate/Character Rate Selection

The S' digit of each OPR instruction issued to the TermiNet Printer Controller specifies the baud rate at which data are to be transferred and the character rate of the device (300 baud = 30 characters per second and 1200 baud - 120 characters per second). When connected to a TermiNet 300 Printer, OPR S' = 0 specifies operation at 300 baud, and when connected to a TermiNet 1200 Printer, OPR S' = 1 specifies operation at 1200 baud. The character rate switch on the printer must be placed in the appropriate position before each message transfer begins.

8.2.4 Additional Features

Device Addresses and API's; the TermiNet controller on the GENIE Bus uses two device addresses (input and output) and generates four API's (two data exchange, two end-of-record) (see 4.3.1).

Alarms; JNE S' = 0 detects device out-of-service conditions and any of the JNE S' = 6 detected alarms. JNE S' = 6 detects input timing errors, parity errors, and device off line when addressed to the input channel. JNE S' = 6 addressed to the output channel detects device off line during output transfers. The alarms detectable by JNE S' = 6 set the controller alarm flip-flop and light the Alarm indicator on the Programming and Maintenance Console.*

Certain alarm conditions transmit a momentary or continuous break to the computer. A break is detectable by noting that the input channel stays perpetually busy in spite of any instructions issued to it. Additional alarm information is provided in the Computer Interface descriptions under 8.2.1 Equipment Options.

Physical Features (Approximate):

1. TermiNet 300 RO Printer - 7.5" H x 20.5" W x 22" D (11.5" H x 20.5" W x 27.3" D with paper handler).

2. TermiNet 300 KSR Printer - 7.5" H x 20.5" W x 26.5" D (11.5" H x 20.5" W x 31.8" D with paper handler).

3. TermiNet 1200 RO Printer - 11.5" H x 20.5" W x 27.3" D, including external paper handler.

4. TermiNet 1200 KSR Printer - 11.5" H x 20.5" W x 31.8" D, including external paper handler.

*A JNE S' = 2 instructions addressed to the receiver or transmitter results in "no jump" if a momentary break is received from the printer.

6. A KSR or RO printer may be separated from the cabinet containing the controller on GENIE Bus that drives it by up to 50 feet of cable when directly connected using the voltage interface. The current loop interface option permits connection by up to 2000 feet of cable. When using a data set at the computer site and a printer with an integral modem, the distance limitation is determined by the communications medium (typically leased phone lines).

Power Requirements:

1. TermiNet 300 RO or KSR Printer - 117 Vac ±10%, 60 Hz, +1 Hz, -1.5 Hz, 185 Watts max. Optional 225 Vac ±10%, 50 Hz ±1%.

2. TermiNet 1200 RO or KSR Printer - 117 Vac ±10%, 60 Hz, +1 Hz, -1.5 Hz, 2.5 Amps max. Optional 225 Vac ±10%, 50 Hz +1%.

Environmental Classes; TermiNet Printers - C. AXSP1 Controller - A (AXSP1 Data Terminal Interface) (See 3.1.)

Controller on GENIE I/O Bus; AXSPI Data Terminal Interface.

8.3 LINE PRINTER

Line Printer model ALPN2 is a high-speed printer available in both standard and quiet cabinet versions that prints up to 600 136-character lines per minute on fan-folded paper up to 16.5 inches wide. The printer uses a drum printing mechanism with which the individual characters on each line are impact printed, as they are read from the printer's memory, and as the desired character in the correct position on the line, rotates under the print hammers.

These printers are available in the following models:

Model	Lines/ Min	Char.	Power	Comments
ALPN21	240	96	60 Hz	
ALPN22	300	64	60 Hz	
ALPN23	436	96	60 Hz	Quiet
ALPN24	600	64	60 Hz	Quiet
ALPN25	240	96	50 Hz	
ALPN26	300	64	50 Hz	
ALPN27	436	96	50 Hz	Quiet
ALPN28	600	64	50 Hz	Quiet

8.3.1 Operating Features

This line printer is a high-reliability, continuous duty unit that prints on fan-folded paper of up to six parts to provide an original and up to five copies. It features an enclosure with a window that allows the print to be viewed as it is printed. Convenient operating controls are provided to the right of the window for applying power, placing the printer on line with the computer, selecting vertical spacing, and advancing the paper.

Printer Characteristics; the printer accepts double-sprocketed paper from 4" to 16.75" in width. The folded sheets may be from 4" to 24" long. Horizontal spacing is 10 characters per inch and vertical spacing is either six or eight lines per inch, as selected by a control panel switch. Vertical paper movement is 10 inches per second for moves up to five lines and 20 inches per second for longer moves, with the final five lines at 10 ips.

Data Format; the first character transferred from the Central Processor to the printer drive is a vertical format code. This is followed by up to 136 printable ASCII characters. The 64-character set includes the upper case alphacharacters, numerals, and punctuation marks. The 96-character set includes the same characters plus the lower case alphabet. Data are transferred to the printer on seven parallel data bit lines.

Vertical format codes 000_8 through 013_8 specify a vertical paper feed to channels 1 through 12 of the vertical format, respectively. Vertical format codes 41_8 through 177_8 specify paper advance of one line through 63 lines, respectively, and 040_8 specifies no paper feed. While the vertical format code is transferred to the printer drive with the OPR instruction that initiates the printing of a line, the drive transfers the format code to the printer with the print instruction and the paper is advanced after the line is printed.

8.3.2 Printing Sequence

1. The program places the vertical format code in the A Register and executes OPR addressed to the printer. The vertical format code is transferred to the printer drive, the drive goes busy, and the first data exchange interrupt is generated.

2. The program transfers each of up to 136 characters to be printed on the line via TOM or OUT, and the characters are retained in the printer's memory.

3. The program transfers DC4 (024_8) via TOM or OUT. This is decoded by the drive board as the print command, and the drive then applies the vertical format code to the printer, followed by the print instruction. The line is printed and the paper is fed according to the vertical format code. The drive goes not busy as the print command is transferred to the printer.

4. When the printer drive goes not busy an end-of-record API is generated.

8.3.3 Additional Features

Device Addresses and API's; the Line Printer Drive on the GENIE I/O Bus uses one device address and generates two API's (data exchange and end-of-record).

Alarms (detected by JNE); printer off line (JNE S' = 0). The printer switches off line when any of the following conditions occurs; hammer misfire, hammer fuse blown, low paper supply, power off. JNE also detects an error if the printer is disconnected from the drive.

Physical Dimensions (approximate); 22" D x 52" W x 45" H, 330 lbs.

Power Requirements; 115 Vac ±10%, 60 Hz ±2% (optional 50 Hz ±2%), 700 Watts maximum.

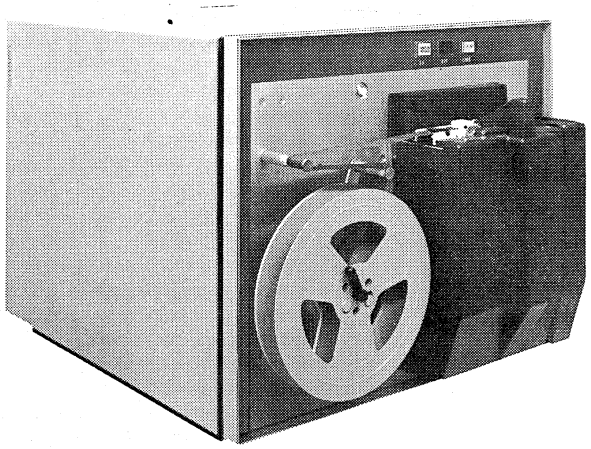
Environmental Classes; AXLP1 Line Printer Drive - A. Line Printer - C. See 3.1

Distance from Controller; the line printer and the drive may be separated by up to 240 feet of cable.

Controller on GENIE I/O Bus; AXLP1 Line printer Drive.

* This product is no longer available as a standard product for new systems or expansions to existing systems.

8.4 PAPER TAPE PUNCH *



The paper tape punch records data characters transferred from the Central Processor on standard one-inch paper tape. A tape handler including a take-up spooler is provided. Model APTP21 uses 60 Hz primary power and model APTP22 is for use on 50 Hz power.

8.4.1 Operating Features

Punching Rate; 120 character (frames per second).

Punch Features; the punch accepts up to 1000 feet of 1.00 ±0.003 inch width and 0.004 ±0.0003 inch thickness. Either dry or oiled paper tape is suitable. The punch punches eight channels per character, ten characters per inch. The punch is ready for operation approximately 0.5 seconds after primary power is applied.

Character Format; data are transferred via the memory (TOM) or from the A Register (OUT) in the Arithmetic Unit to the tape as shown on Fig. 8-1.

8.4.2 Record Format

1. The program executes an OPR instruction with S' = 0 to specify ASCII format or with S' = 1 to specify EIA RS-244 format.

2. The program transfers STX (002_8) via TOM or OUT if using ASCII mode. STX is punched on the tape.

3. Program transfers text characters via TOM or OUT. Characters are punched.

4. ETX (033_8) and DC3 (023_8) are normally added after the text to permit proper operation of the tape on the paper tape reader (ASCII mode).

5. To maintain compatibility with teletypewriter tapes, program may transfer CR (015_8) and LF (012_8) after DC3.

6. Program transfers DC4 (024_8) is using ASCII, or DEL (177_8) is using EIA. End-of-record API is generated. DC4 is punched. DEL is not punched.

7. NUL (000_8) may precede or follow any tape record to serve as a tape leader. NUL is merely a frame consisting of a sprocket hole only (no data holes).

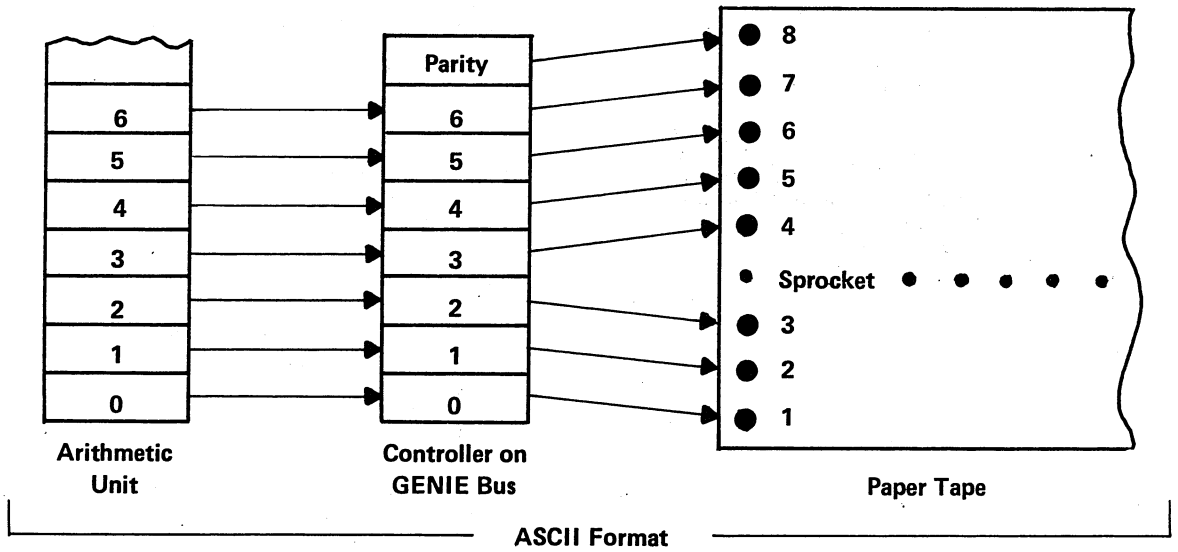
8.4.3 Additional Features

Device Address and API's; the punch controller on the GENIE Bus uses one device address and generates two API's (data exchange and end-of-record).

Alarms (detected by JNE); punch off line (JNE S' = 0); out of tape or broken tape (JNE S' = 2).

Physical Dimensions (approximate); 19.5" W x 17.4" H x 28" D.

Power Requirements; 115 Vac ±10%, approximately 10 Amps starting current and 3.5 Amps running current.



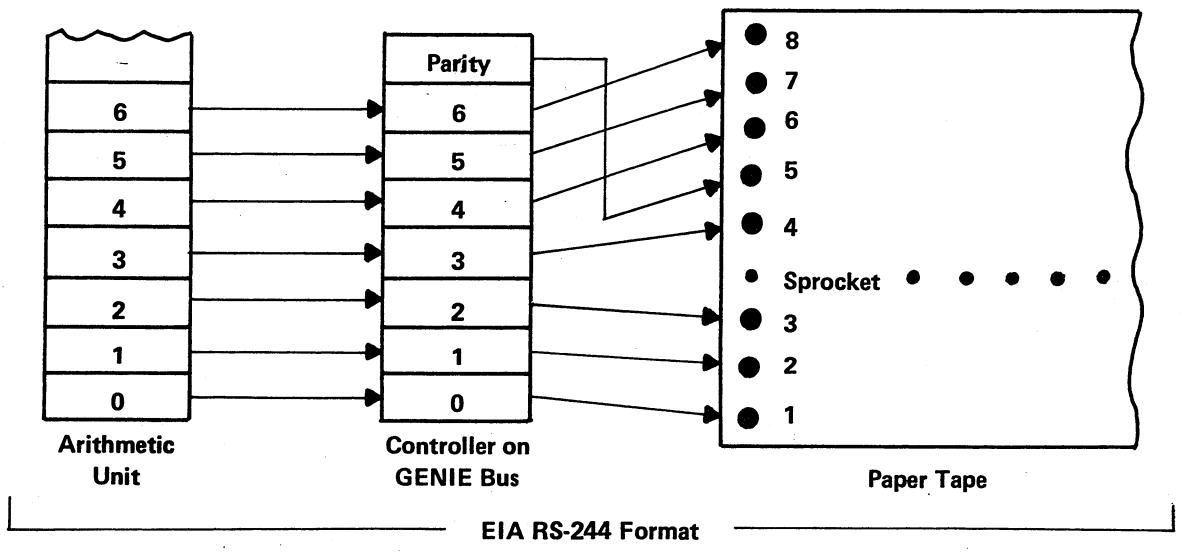


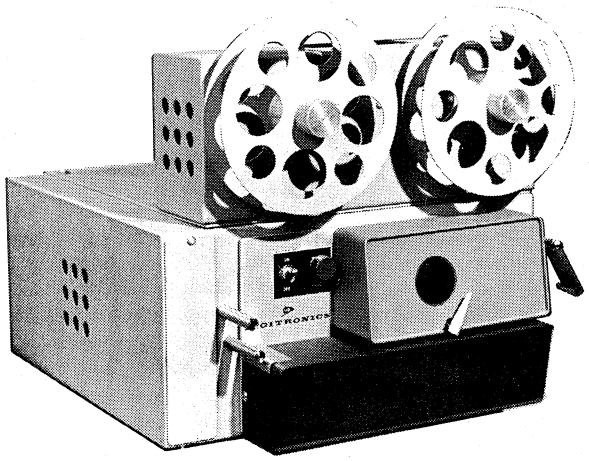
Fig. 8-1 Punched Tape Formats

Environmental Classes; Paper Tape Punch - C, AXPP1 Controller A. (See 3.1.)

Distance from Controller; the paper tape punch and the controller may be separated by up to 500 feet of cable.

Controller on GENIE I/O Bus; AXPP1 Card/Tape Punch Drive.

8.5 PAPER TAPE READER *



The paper tape reader reads data characters from paper tape, metalized plastic tape, or plastic-backed paper tape. A tape handler, including a supply reel and take-up spooler, is provided. Model APTR21 uses 60 Hz primary power and model APTR22 is for use on 50 Hz power.

* This product is no longer available as a standard product for new systems or expansions to existing systems.

8.5.1 Operating Features

Speed; 100 characters (frames) per second. The reader is free-running, is started by the program, and stops on detection of an end-of-record character as read from the tape.

Reader Features; the reader accepts one-inch wide tape of 0.004 to 0.005 inch thickness. The photo-electric reader reads eight-channel, ten-characters -per-inch tapes. Rewind speed is nominally 100 inches per second. The reader is ready for operation approximately one second after power is applied. The take-up and supply reels hold approximately 300 feet of tape with a hub and 500 feet without a hub. Tape is normally supplied on a plastic hub which slips onto the reel assembly.

Character Format; data are transferred from the tape through the controller to the Arithmetic Unit as shown on Fig. 8-2.

8.5.2 Record Format

1. The program transfers DC1 (021_8) via OPR. The reader is started.

2. The first character in the tape record should be STX (002_8). Upon detection of STX, the generation of data exchange API's is enabled. STX is not transferred to the Arithmetic Unit.

3. Text characters are read from the tape and transferred to the Arithmetic Unit via TIM or IN.

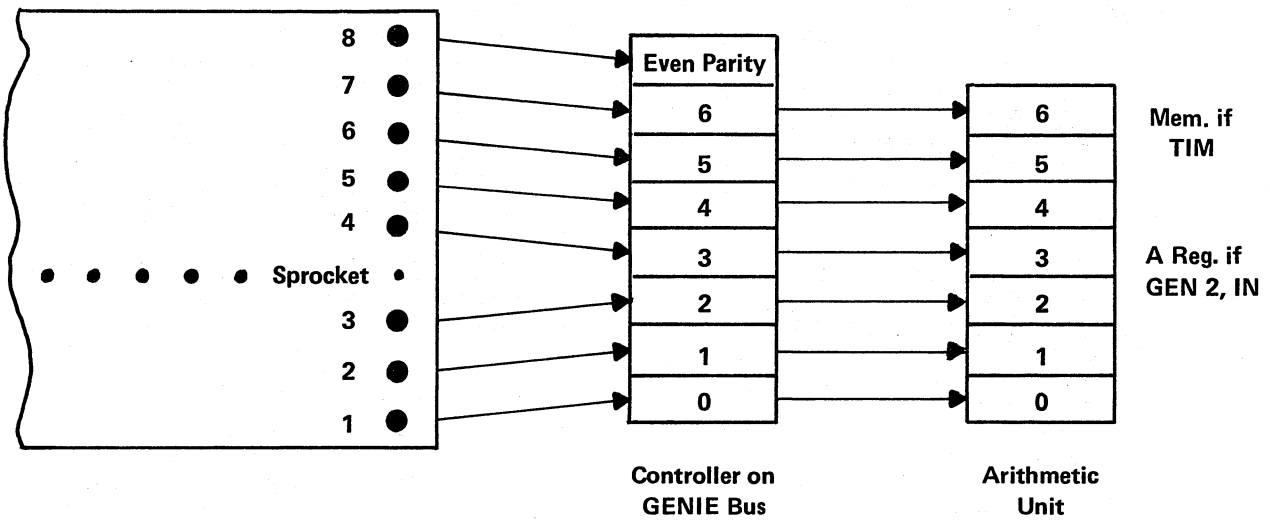


Fig. 8-2 Reader Tape Format

4. ETX (003_8) normally follows the last text character on the tape and is transferred to the Arithmetic Unit.

5. DC3 (023_8) is read from the tape. Upon detection of DC3, the reader is turned off and an end-of-record API generated.

8.5.3 Additional Features

Device Address and API's; the reader controller on the GENIE Bus uses one device address and generates two API's (data exchange and end-of-record).

Alarms (detected by JNE); reader disconnected (JNE S' = 0); power off, out of tape, or broken tape (JNE S' = 2), parity or timing error (JNE S' = 6).

Physical Dimensions (approximate); 13.8" D x 19.3" W x 13.3" H. Four inches minimum are required at the reader to accommodate a cable connector.

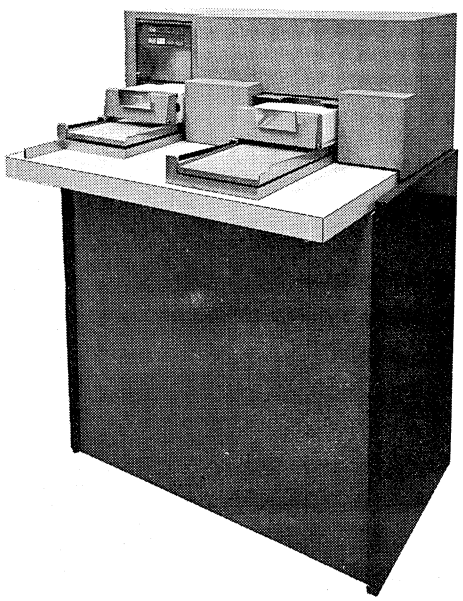
Power Requirements; 115 Vac ±10%, 125 Watts nominal, 1.5 Amps nominal running current.

Environmental Classes; Paper Tape Reader and AXPR1 Controller A. See 3.1.

Distance from Controller; the reader and the controller may be separated by up to 500 feet of cable.

Controller on GENIE I/O Bus; AXPR1 Card/Tape Reader Controller.

8.6 CARD PUNCH



* This product is no longer available as a standard product for new systems or expansions to existing systems.

The card punch records data half-words transferred from the Central Processor on standard 80-column, 12-row computer data cards. Data are punched column-by-column. Each column contains one 12-bit data half-word. Model ACDP21 uses 60 Hz primary power and model ACDP22 uses 50 Hz power.

8.6.1 Operating Features

Punching Rate; varies by the number of columns punched on each card. If 80 columns are punched, the rate is 60 cards per minute. If ten or fewer columns are punched, the rate is 200 cards per minute.

Punch Features; cards may be punched in Hollerith or binary codes, as the characters are formed by the program. The input hopper and the output stacker both accommodate 1500 cards. Each column punched is checked by the punch for compliance with the character transferred by TOM or OUT. If the comparison is not correct, a Punch Error lamp on the punch is lit and the JNE error test line goes "true". Each half-character transferred to the punch is checked for correct even parity, but the parity bit is not punched.

Data Format; data characters are transferred to the cards from the memory (TOM) or the A Register (OUT) as shown on Fig. 8-3.

8.6.2 Card Punching Sequence

1. The program initiates a punch operation by executing OPR addressed to the punch controller on the GENIE Bus. During exectuion of OPR, the A Register must contain a number equal to one less than twice the number of columns to be punched. As an example, if 80 columns are to be punched, the A Register must contain $160 - 1 = 159 = 237_8$. The first data exchange API is then generated.

2. The TOM function or OUT transfers the first of two characters required to punch a 12-bit column (Fig. 8-3). The punch is then enabled, and the second data exchange API is generated.

3. TOM or OUT transfers the second half-character. The column is punched and the next data exchange API is generated. Five milliseconds are available to complete steps 2 and 3.

4. Characters continue to be transferred and punched as in steps 2 and 3 until the number of half-characters and columns indicated by the A Register in step 1 have been punched. The punched card is ejected, a new card made ready, and the end-of-record API is generated.

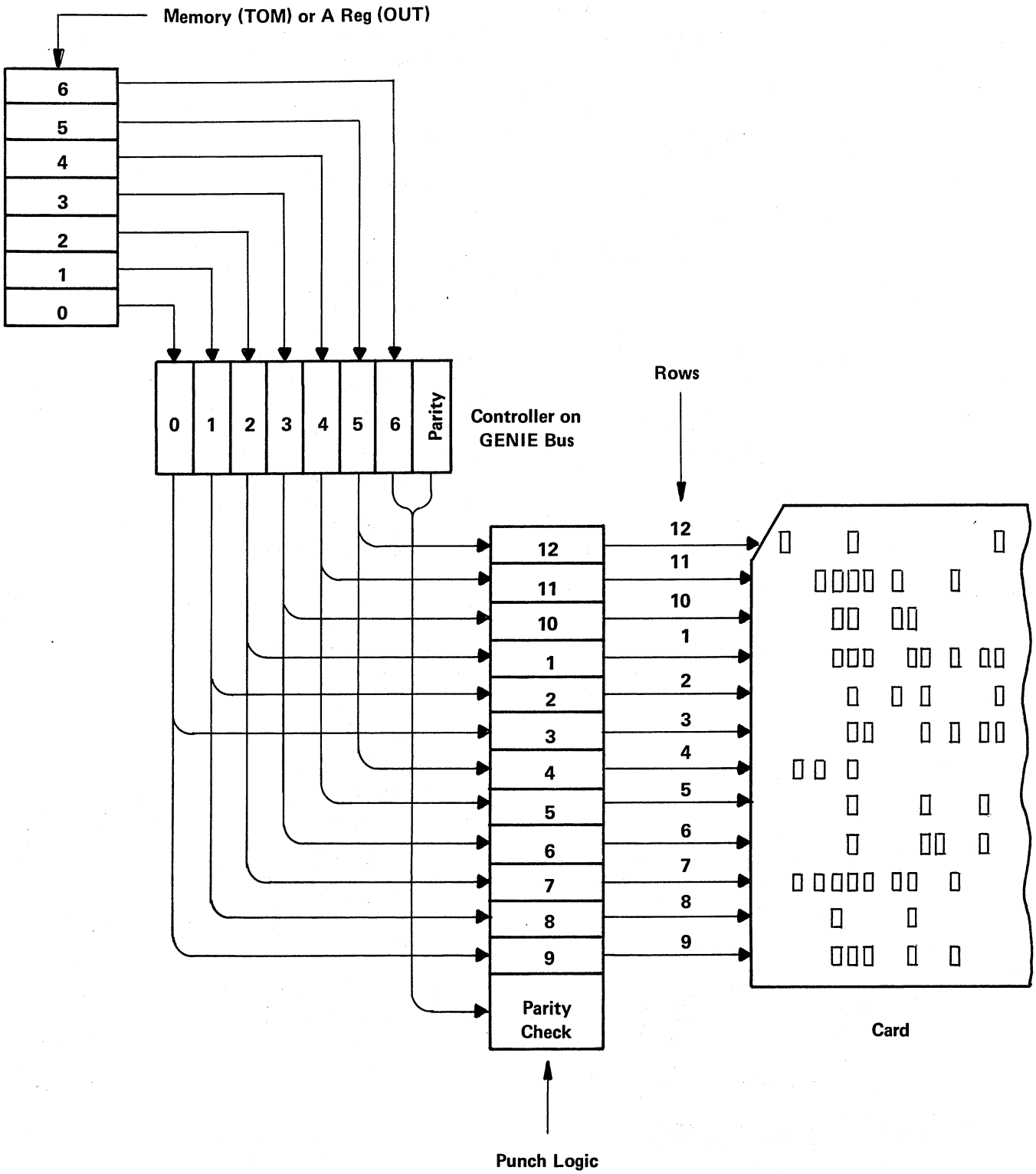


Fig. 8-3 Punched Card Format

8.6.3 Additional Features

Device Address and API's; the punch controller on the GENIE Bus uses one device address and generates two API's (data exchange and end-of-record).

Alarms (detected by JNE); punch halted (off line, mechanical or electrical failure) (JNE S' = 0); punch interlock open, punch error, registration error, or jam (JNE S' = 2); hopper empty or stacker full (JNE S' = 4); data parity error, card ejected late, data transferred too late (JNE S' = 6).

Physical Dimensions (approximate); 49" H x 34" W x 21" D; 550 lbs.

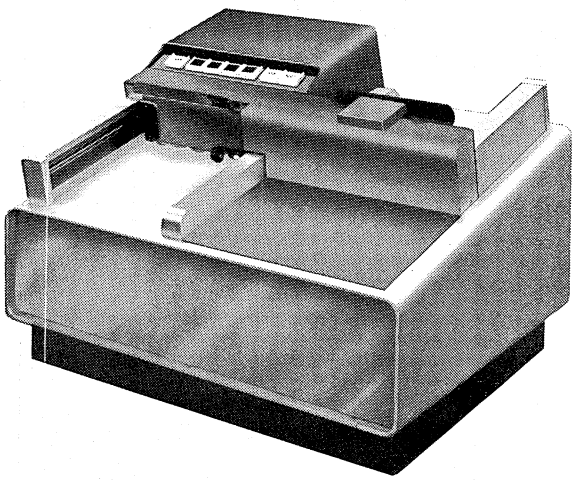
Power Requirements; 115 Vac ±10%, 20 Amps nominal starting current, 7 Amps nominal running current.

Environmental Classes; AXPP1 Controller A, Card Punch - C. (See 3.1.)

Distance from Controller; the punch and the controller may be separated by up to 500 feet of cable.

Controller on GENIE I/O Bus; AXPP1 Card/Tape Punch Drive.

8.7 CARD READER



The card reader senses 12-bit half-words, column-by-column, from standard 80-column computer data cards. The following models are available:

ACDR21 - 300 cards per min., 60 Hz power.

ACDR23 - 300 cards per min., 50 Hz power.

ACDR22 - 600 cards per min., 60 Hz power.

ACDR24 - 600 cards per min., 50 Hz power.

8.7.1 Operating Features

Speed; 300 or 600 cards per minute, according to the model used.

Card Reader Features; the photo-diode reader reads 12-row, 80-column cards. Cards of differing stock may be intermixed. Cards may have a square or cut corner. Cards are air-ruffled for reading and are fed by a vacuum pick device from a 1000-card hopper to a 1000-card stacker. The reader halts automatically when it detects an error.

Data Format; 12-bit half-words are read from the cards and transferred to memory (TIM) or the A Register (IN) as shown on Fig. 8-4.

8.7.2 Card Reading Sequence

1. With the reader on and cards in the hopper, the operator pushes the Demand switch on the reader. If the controller is not busy, it goes busy, then not busy, and an end-of-record API is generated.

2. The program executes an OPR instruction addressed to the controller. The contents of the A Register are ignored, a card is picked, moved into position to read the first column, and the first data exchange API is generated.

3. The program reads the first column and subsequent columns through the TIM function or via IN instructions as the card moves past the read station. As each column is in position to be read, a data exchange API is generated.

4. After the 80th column has been read, the reader senses that the end of the card is near, and an end-of-record API is generated.

8.7.3 Additional Features

Device Address and API's; the reader controller on the GENIE Bus uses one device address and generates two API's (data exchange and end-of-record).

Alarms (detected by JNE); reader off line (JNE S' =0); card feed failure, light or dark check failure (JNE S' =2), hopper empty or stacker full (JNE S' = 4), timing error -

data from next column read before data held by controller is transferred to AU (JNE S' = 6).

Physical Dimensions (approximate); 23" W x 14" H x 22" D; 76 lbs.

Power Requirements; 115 Vac ±10%, 4.6 Amps nominal running current.

Environmental Classes; AXPR1 Card/Tape Reader Controller - A, Card Reader - C. (See 3.1.)

Distance from Controller; the reader and the controller may be separated by up to 500 feet of cable.

Controller on GENIE I/O Bus; AXPR1 Card/Tape Reader Controller.

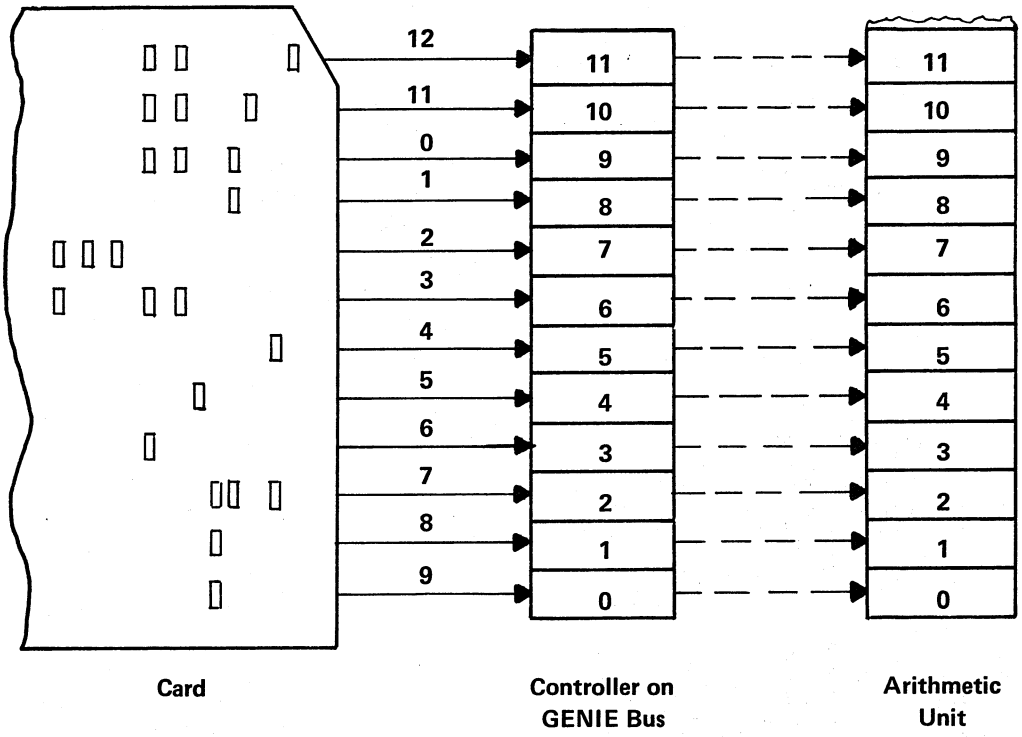


Fig. 8-4 Card Reading Format

8.8 MATRIX PRINTER DEVICE (MPD)

Matrix Printer Devices are used in a system at the computer site, or as remote terminals at distant sites. The first I/0 printer implemented in the system normally serves as the Programming and Maintenance I/0 typer.

Matrix Printer Devices are quiet, compact units, in which most functions are performed electronically, minimizing mechanical functions. Printing is accomplished by means of a seven-needle impact printing head. Printed characters consist of small dots. A 300-baud printer option communicates with the computer and prints 30 characters per second using a 7x9 dot matrix. A 1200-baud printer operates at 120 characters per second with a 7x7 dot matrix.

Both the 300-baud and the 1200-baud printers are available as receive only (RO) devices and as keyboard send and receive devices (KSR), with either a voltage computer interface or a current loop computer interface. The following Matrix Printer models are available:

AMPA21,22 Matrix Printer 300-baud KSR Voltage Interface, 60 Hz, 50 HZ

AMPA23,24 Matrix Printer 300-baud KSR Current Interface, 60 Hz, 50 Hz

AMPA11,12 Matrix Printer 300-baud RO Voltage Interface, 60 Hz, 50 Hz

AMPA13,14 Matrix Printer 300-baud RO Current Interface, 60 Hz, 50 Hz

AMPB21,22 Matrix Printer 1200-baud KSR Voltage Interface, 60 Hz, 50 Hz

AMPB23,24 Matrix Printer 1200-baud KSR Current Interface, 60 Hz, 50 Hz

AMPB11,12 Matrix Printer 1200-baud RO Voltage Interface, 60 Hz, 50 Hz

AMPB13,14 Matrix Printer 1200-baud RO Current Interface, 60 Hz, 50 Hz

8.8.1 Matrix Printer Options

The following descriptions apply to both the 300-baud printer and the 1200-baud printer. These are switch selectable options that are pre-set for RTMOS software compatibility.

Vertical Tabulation and Form-feed Option*

This option is virtually mandatory when fan-folded paper is used. It is designed for paper with an 11-inch form length (66 lines per page). The top-of-form position and the vertical tab positions are specified by holes punched in a special tape by the user. Vertical tabulation can also be set from the computer or the keyboard. A vertical tab code (VT, 013$_8$), transferred from the computer or generated at the keyboard, slews the paper to the top of the next form (page). See the 4500 Computer Operator's Manual, PTS-039, for details on how to set vertical tabs from the computer at the keyboard.

8.8.2 Matrix Printer Features

These features are incorporated in both the 300-baud and the 1200 baud printers.

Parity Error Detection Feature

The Matrix Printer includes a parity error detection feature that prints a diamond when a character with incorrect parity is received from the device's interface. This feature is useful when the printer is located remotely from the computer and the two sites are connected by modems and telephone lines. Even parity, which is compatible with standard asynchronous modem communication format, is used for the check.

Print Visibility

The printing head automatically moves three positions beyond the current print position after at least 0.8 seconds of no printing activity. The printing head is three positions to the left of the first print position when a carriage return is completed, providing print visibility at all times.

*This option is not supported by the standard RTMOS software. The user must insert the proper codes and fill characters in his data string before making an output call to RTMOS.

Horizontal Tabulation

The horizontal tab positions can be set at the current character position from the keyboard or by transferring ESC (033$_8$) followed by 1 (061$_8$) from the computer. A horizontal tab code (HT, 011$_8$) generated at the keyboard or transferred from the computer moves the current character position to the next tab position. All tabs are cleared on loss of power.

Paper Out Sensor

A sensor on the left tractor detects that the form supply is depleted. When a paper-out condition is detected, the device stops printing, the STAND-BY indicator lights, and the "Data Terminal Ready" and "Request to Send" computer interface signals are true.

Automatic New Line

The printer automatically performs carriage return/line feed when the printing head is at the end of a print line and characters are received without CR and LF.

Audible Alarm

An audible alarm activates for about 0.5 seconds when a BEL command is received from the computer or keyboard.

Print Line Length and Paper Feed

The print line length is a maximum of 132 characters. The printers feature pin-feed tractors that can be adjusted to accept any paper width from 4 inches to 15 inches, with 12-11/32 inches pin-to-pin spacing.

Computer Interfaces

Where the computer and the printer can be connected by up to 50 feet of cable, a voltage interface is used for direct connection to the printer. Where the computer and the printer sites are separated by a considerable distance, a modem interface to a modem connected to the printer may be used. In both cases, the printer and the computer interfaces comply with EIA standard RS-232C.

A direct connection with up to 2000 feet of cable may be made when the current loop interface is used. This interface returns alarm status to the computer as is returned over the voltage or modem interfaces. This interface also returns a continuous break signal on the input line to the computer when the printer is in the local mode, has ac power off, or is not connected to the computer. This continuous break condition may be detected by JNE S' = 0 addresses to the input channel (see Alarms under 8.8.5).

Both interfaces return a momentary break to the computer when a printer alarm occurs or when the BRK button on the printer is pushed. The momentary break sets the alarm flip-flop in the controller and the alarm line may be tested by JNE S' = 6 addressed to the input channel (see Alarms under 8.8.5).

8.8.3 Operating Features

The printer prints all printable characters in the ASCII character set (see Table 8-1), including both upper and lower case letters. The keyboard is capable of generating all 128 ASCII codes, including all printable characters. The computer programs, however, typically recognize and transmit only upper case letters, so a switch on the printer is pre-set to cause transmission of the upper case code when a letter key is pushed with or without pushing the SHIFT key.

Horizontal character spacing is 10 characters to the inch, and vertical line spacing is six lines per inch. The printer is capable of printing up to a five-part form (one original and four copies). The ribbon is a cartridge type, which may be easily replaced by the operator.

Character exchanges between the computer and the printer are bit-serial asynchronous at either 300 baud or 1200 baud, depending on the model. A full-duplex communications link is used, and when the printer is on-line with the computer it does not directly print characters transmitted to the computer, but prints the characters as they are "echoed" back to the printer from the I/O Buffer control in the computer. The printer recognizes characters from the computer only when on-line, and responds to locally generated printing and control characters only when in the local mode. Each serial character exchanged between the computer and the printer consists of a start bit, seven data bits, an even parity bit, and one stop bit, or a total of ten serial bits. The least significant data bit is moved first, and the data lines remain in the marking state in the absence of any data transmissions, as long as the printer remains on-line.

Octal Code	Character	Keys	Octal Code	Character
000	NUL	CTL, @	040	SP
001	SOH	CTL, A	041	!
002	STX	CTL, B	042	"
003	ETX	CTL, C	043	#
004	ETO	CTL, D	044	$
005	ENQ	CTL, E	045	%
006	ACK	CTL, F	046	&
007	BEL	CTL, G	047	'
010	BS	CTL, H	050	(
011	HT	CTL, I	051	)
012	LF	CTL, J	052	*
013	VT	CTL, K	053	+
014	FF	CTL, L	054	,
015	CR	CTL, M	055	-
016	SO	CTL, N	056	.
017	SI	CTL, O	057	/
020	DLE	CTL, P	060	0
021	DC1	CTL, Q	061	1
022	DC2	CTL, R	062	2
023	DC3	CTL, S	063	3
024	DC4	CTL, T	064	4
025	NAK	CTL, U	065	5
026	SYN	CTL, V	066	6
027	ETB	CTL, W	067	7
030	CAN	CTL, X	070	8
031	EM	CTL, Y	071	9
032	SUB	CTL, Z	072	:
033	ESC	ESC	073	;
034	FS	CTL, \	074	<
035	GS	CTL,]	075	=
036	RS	CTL, ~	076	>
037	US	CTL, US	077	?

Table 8-1 United States ASCII Code Character Set

(continued on next page)

(continued)

Octal Code	Character	Octal Code	Character
100	@	140	(Space)
101	A	141	a
102	B	142	b
103	C	143	c
104	D	144	d
105	E	145	e
106	F	146	f
107	G	147	g
110	H	150	h
111	I	151	i
112	J	152	j
113	K	153	k
114	L	154	l
115	M	155	m
116	N	156	n
117	O	157	o
120	P	160	p
121	Q	161	q
122	R	162	r
123	S	163	s
124	T	164	t
125	U	165	u
126	V	166	v
127	W	167	w
130	X	170	x
131	Y	171	y
132	Z	172	z
133	[	173	{
134	\	174	¦
135	]	175	}
136	^	176	~
137	←	177	DEL

Table 8-1 United States ASCII Code Character Set

All versions of the printer provide a buffer to eliminate or reduce the need for fill characters. Characters coming from the modem interface are loaded into the buffer when the mechanism cannot accept a print command. All characters coming from the line with buffer overflow are lost. The 300-baud printers have a buffer that holds 64 characters and the 1200-baud printers have a 1000-character buffer capacity.

For detailed descriptions of the operating controls, refer to the 4500 Computer Operator's Manual, PTS-039.

8.8.4 Message Formats

The following descriptions cover the effect of various control codes and the basic message sequences and characters.

Control Codes

The following is a summary of the control codes that the printer responds to within the software programs:

BEL	Activates an audible alarm for about 0.5 seconds.
BS	Moves the printing head one position to the left.
HT	Moves the printing head forward to the next tab position. If no tabs have been set, the head moves to the end of the line.
LF	Advances the paper one line.
VT	Advances the paper up to the next vertical tab, or to the first line of the next sheet when tabs have not been set.
FF	Advances the paper to the first line of the next sheet.
CR	Moves the printing head to the first tab or to the first print position when no tabs have been set.
ESC, 1*	Sets a horizontal tab at the current position.
ESC,2	Clears all horizontal tabs (all tabs are cleared at power-on).
ESC, 3	Sets a vertical tab at the current line.
ESC, 4	Clears all vertical tabs.
ESC, 0	Plus X character (see 4500 Computer Operator's Manual, PTS-039) determines the page length. The printer is initially set for 66 lines, but the maximum page length is 126 lines.
ESC, H (ESC, h)	Switches the printer to ON-LINE status from the STAND-BY status.
ESC, J (ESC, j)	Switches the printer to STAND-BY status from the ON-LINE status.
ENQ	Results in the answer of an ACK code when the printer is in READY status, and a NACK code when the printer is in STAND-BY status.

Output to Printer

To initiate operation, the program executes an Operate instruction addressed to the out-put controller on the GENIE Bus with 117$_8$ in the A Register. The output channel goes busy, the 177$_8$ character is not transferred to the printer, and the first data exchange interrupt occurs. The program then transfers the two on-line status characters (ESC, H) if needed, and then transfers the text characters. The final text character is followed by CR, LF, the stand-by status characters (ESC,J) may then be transferred, and the program transfers DC4, which sets the channel not busy and generates the end-of-record interrupt.

Keyboard Input

The operator pushes the BREAK button on the printer, which transmits a momentary break signal to the computer that makes the controller input channel go busy and then not busy, generating an end-of-record interrupt. The program then executes an Operate instruction addressed to the

*This notation means ESC followed by the numeral or letter.

input channel with STX in the A Register. OPR sets the input channel busy and STX enables the echo-net function. As the operator strikes each key to transmit a character, the data exchange interrupt is requested when the complete character is held in the input holding register. The characters are input until the operator strikes the Return key, which generates CR. When CR is input, the input channel goes not busy and the end-of record interrupt is requested.

Baud Rate Selection

The S' digit of each OPR instruction issued to the Matrix Printer Controller specifies the baud rate at which data are to be transferred and the character rate of the device (300 baud = 30 characters per second and 1200 baud = 120 characters per second). When connected to a 300 printer, OPR S' = 0 specifies operation at 300 baud, and when connected to a 1200 printer, OPR S' = 1 specifies operation at 1200 baud.

8.8.5 Additional Features

Device Addresses and API's

The Matrix Printer controller on GENIE Bus uses two device addresses (input and output) and generates four API's (two exchange, two end-of-record) (see 4.3.1).

Alarms

JNE S' = 0 detects out-of-service conditions and any of the JNE S' = 6 detected alarms. JNE S' = 6 detects input timing errors, parity errors, and device off-line when addressed to the input channel. JNE S' = 6 addressed to the output channel detects device off-line during output transfers. The alarms detectable by JNE S' = 6 set the controller alarm flip-flop and light the Alarm indicator on the Programming and Maintenance Console.*

Non-operable alarm conditions transmit a momentary or continuous break to the computer. A break is detectable by noting that the input channel stays perpetually busy in spite of any instructions issued to it.

Physical Features (Approximate)

1. 300 RO and 1200 RO Matrix Printers - 190.5 mm (7.5") H x 590 mm (23") W x 520 mm (20.5") D.
2. 300 KSR and 1200 KSR Matrix Printers - 190.5 mm (7.5") H x 590 mm (23") W x 660 mm (26") D.

Power Requirements

All Models -	115 Vac ±10%, 60 Hz**
	115 Vac ± 10%, 50 Hz**
	318 VA max. power

Environmental Class

Matrix Printer -	Class C
Controller -	Class A

*A JNE S' = 2 instruction addressed to the receiver or transmitter results in "no jump" if a momentary break is received from the printer.

**The printers may be converted for either power frequency option per instructions provided in the Honeywell maintenance procedures.

HONEYWELL PROCESS VIDEO (HPV-2) DISPLAY SUBSYSTEM

The HPV-2 Honeywell Process Video Display Subsystem (High Performance Video), provides a significantly improved and highly effective human interface to process automation. By employing new techniques, the HPV-2 provides many features not available on previous video display subsystems. These features enable the process operators and/or plant engineers to interact effectively with complex processes or distribution systems.

The HPV-2 performs the function of a communications link between the operator and the control system. To enhance the extraction of information from the system, the HPV-2 features: Alphanumeric Character Sets which are oriented toward Process Control Systems, Data Trending which produces a display of data in a format similar to that of a strip chart recorder, Character Scaling for added visibility at a greater distance from the display, Reverse Field to emphasize the characters displayed, and Reduced Intensity to add varying degrees of importance to the information.

To simplify the input of information to the computer system, the HPV-2 offers a keyboard with 54 keys for entering the alphanumeric or graphic data, 26 control keys, 5 cursor controls, and 10 numeric keys. A 45-function key option is also available. In addition to the keyboard, the Light Pen, an optional cursor positioning device, may be incorporated into the subsystem.

The HPV-2 Subsystem consists of a Computer Interface Controller (high speed parallel or asynchronous serial), a Display Generator containing from one to four Channel Sets, Display Monitors (one primary with up to four optional slaves per channel), optional keyboard, and an optional Light Pen as shown in Fig. 9-1.

9.1 OPTIONS

9.1.1 Display Generator Options

The Honeywell Process Video Display Generator contains from one to four Channel Sets consisting of the memory and logic necessary to store the information on one separately addressable display and to generate the video display. Channel Sets can be added to Display Generators by plugging in the necessary printed wire boards.

The Display Generator chassis contains the common logic and one to four Channel Sets. The Display Generator can be ordered with one or two computer ports. The computer interface is either a local (parallel) or remote (serial) Video Interface Controller which connects on the GENIE I/O Bus.

The Display Generator's common logic consists of an Interface Board, a Microprocessor Board, and a Sync Generator Board. Dual port systems require an additional Interface Board and Microprocessor Board for Port B.

There are two basic Channel Sets available: The Alphanumeric Channel Set and the Trend Channel Set. The Alphanumeric Channel Set is available in two versions; one with a SEER graphics character set and another with a SCADA graphics character set. Both Alphanumeric Channel Sets feature character blinking, character protect, reverse color, reduced intensity, and character scaling.

The Display Generator model numbers to include channel set options are:

4DP3AAPVxyz, where:

APVB11	One HPV-2 Parallel Video Interface
APVB12	One HPV-2 Serial Video Interface
APVC__	Display Generator w/Single Parallel Interface
APVD__	Display Generator w/Dual Parallel Interface
APVF__	Display Generator w/Single Asynchronous Interface
APV_1_	One SCADA or PM/C Alphanumeric Channel Set
APV_2_	Two SCADA or PM/C Alphanumeric Channel Sets
APV_3_	Three SCADA or PMC Alphanumeric Channel Sets
APV_4_	Four SCADA or PM/C Alphanumeric Channel Sets
APV_5_	One SEER Alphanumeric Channel Set
APV_6_	Two SEER Alphanumeric Channel Sets

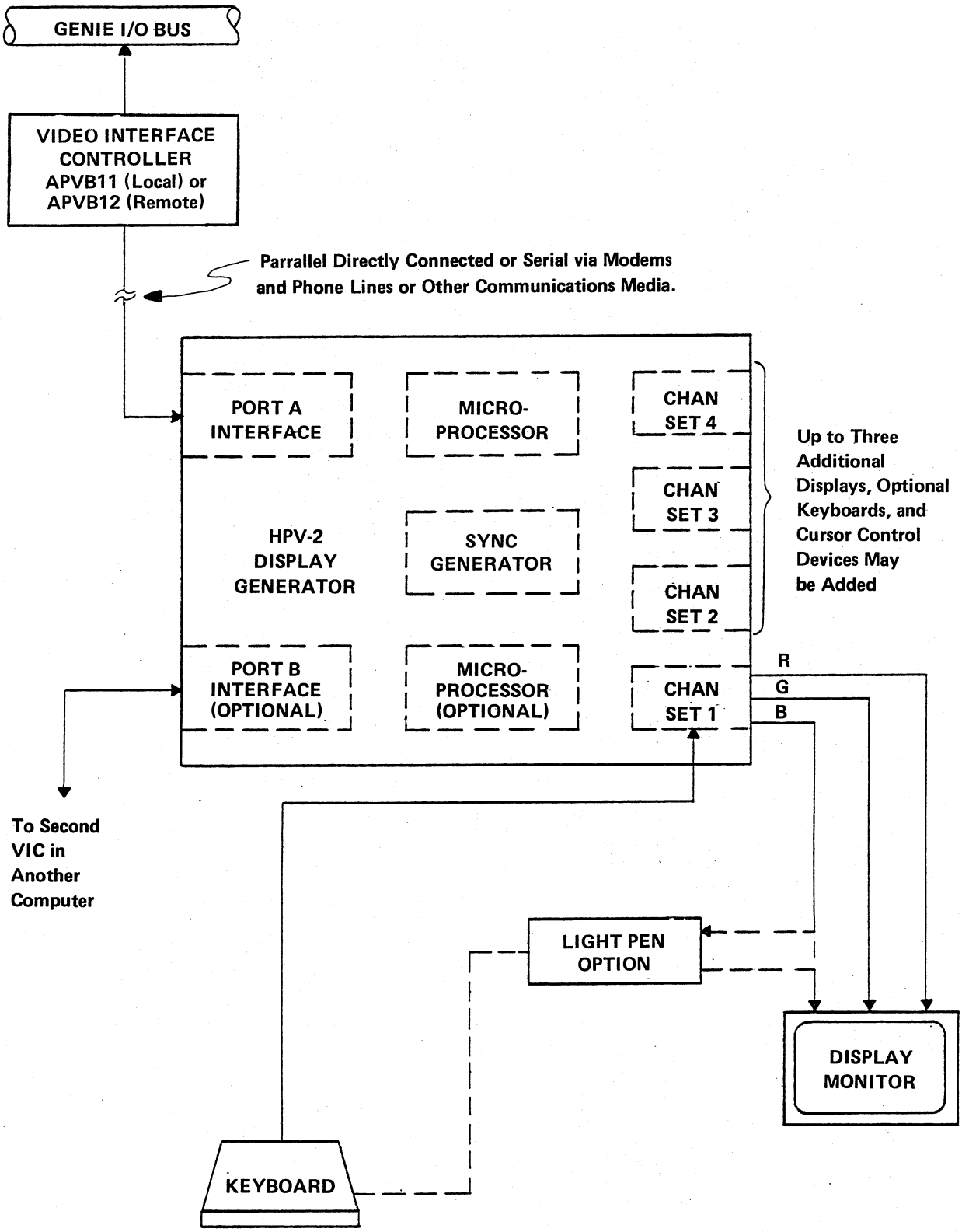


Fig. 9-1 HPV-2 Subsystem

APV_7_	Three SEER Alphanumeric Channel Sets
APV_8_	Four SEER Alphanumeric Channel Sets
APV__0	No SEER or SCADA TREND Channel Sets
APV__1	One SEER or SCADA TREND Channel Set
APV__2	Two SEER or SCADA TREND Channel Sets
APV__3	No PM/C TREND Channel Sets
APV__4	One PM/C TREND Channel Set
APV__5	Two PM/C TREND Channel Sets

NOTE

The Display Generator accommodates up to four Channel Sets. Each Trend Channel Set requires a corresponding Alphanumeric Channel Set.

Character Sets. A total of 128 display symbols are produced by the video generation logic in each Alphanumeric Channel Set. Of these 128 sybmols, 64 are alphanumeric and punctuation characters, four are tab, cursor, and field selection characters, and 60 are graphic symbols. Three standard Alphanumeric Channel Set types are available for use with three Honeywell product systems: SEER, SCADA, and PM/C.* Other graphic character sets can be custom designed, at additional cost, to meet the needs of special applications. Once programmed, the character generator PROMs cannot be reprogrammed.

In addition to the Alphanumeric Channel Sets, Data Trend Channel Sets can be supplied for those applications which require data to be displayed in a format similar to a strip chart recorder. Note that the Trend Channel Sets require an Alphanumeric Channel Set to supply the alphanumeric characters required to notate the charts.

9.1.2 Display Monitors

The Display Monitors are high resolution, highly stable units, with excellent linearity. While all Channel Sets generate video output characters in seven colors, each also has a monochrome (black and white) video output. The standdard color monitors have 19" or 25" diagonally measured screens and feature a black matrix CRT for superior resolution and contrast. See Fig. 9-2.

Model numbers for the monitors are as follows:

APVB71	19" Color Rack Mount 60 Hz
APVB72	19" Color Desk Mount 60 Hz
APVB73	19" Color Yoke Mount 60 Hz
APVB74	19" Color Rack Mount 50 Hz
APVB75	19" Color Desk Mount 50 Hz
APVB76	19" Color Yoke Mount 50 Hz
APVB77	19" Color Modular Furniture Mount 60 Hz
APBV78	19" Color Modular Furniture Mount 50 Hz
APVB81	25" Color Desk Mount 60 Hz
APVB82	25" Color Yoke Mount 60 Hz
APVB83	25" Color Desk Mount 50 Hz
APVB84	25" Color Yoke Mount 50 Hz

NOTE

Model numbers listed apply to CONRAC Model 5111 Monitors. For CONRAC Model 5211 Monitors, change the model numbers from APVB___ to APVK___.

The maximum length of the coaxial cables between the Display Generator and the Display Monitors (three for color) is 300 ft.

9.1.3 General Purpose Keyboards

Each of the four possible alphanumeric display channels in a Display Generator may be served by a compatible keyboard. Standard keys are alphanumeric keys, punctuation keys, cursor control keys, color switch keys, edit function

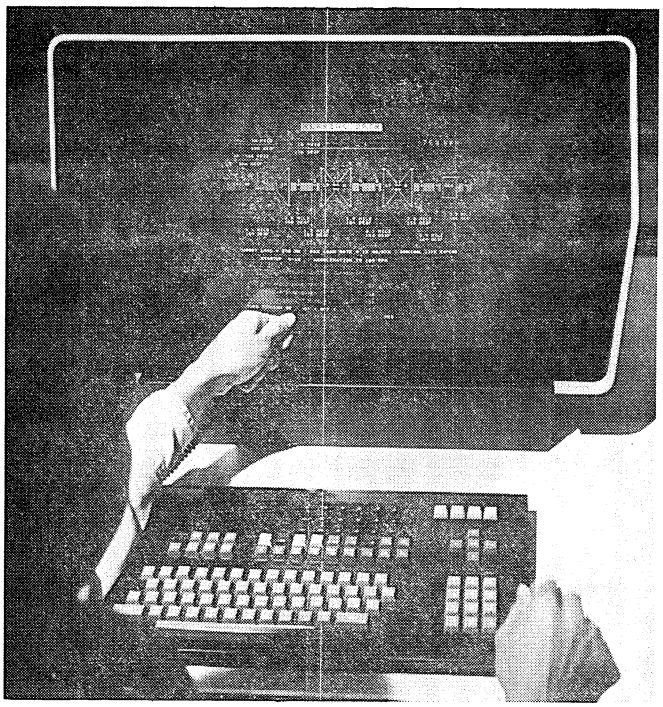


Fig. 9-2 19" Color Monitor With Keyboard in Modular Furniture

* Refer to theory publication APVB-J-T for descriptions of the standard character sets.

keys, transmit data keys, and a 10-numeral keypad. In addition a 45-key function code option is available. The function key option has 45 function keys plus two double-size "enable" keys. The operator can transmit a function code to the computer by holding the enable key down and then pressing the desired function key. The computer software recognizes the function code as specifying that a predetermined system function is requested by the operator. Through the use of simultaneous dual keystrokes, large characters and graphic characters may be entered on the display. The graphic characters are engraved on the appropriate alphanumeric keys. A typical keyboard is shown in Fig. 9-3.

Keyboard model numbers and options are as follows:

APVB41	SEER, no function keys, with case
APVB42	SEER, no function keys, without case
APVB43	SEER, 45 function keys, with case
APVB44	SEER, 45 function keys, without case
APVB45	SEER, no function keys, with case, with light pen
APVB46	SEER, no function keys, without case, with light pen
APVB47	SEER, 45 function keys, with case, with light pen
APVB48	SEER, 45 function keys, without case, with light pen
APVB51	SCADA, no function keys, with case
APVB52	SCADA, no function keys, without case
APVB53	SCADA, 45 function keys, with case
APVB54	SCADA, 45 function keys, without case
APVB55	SCADA, no function keys, with case, with light pen
APVB56	SCADA, no function keys, without case, with light pen
APVB57	SCADA, 45 function keys, with case, with light pen
APVB58	SCADA, 45 function keys, without case, with light pen
APVB62	Flush mount for no function keys
APVB63	Flush mount for 45 function keys
APVB64	Modular furniture mount for no function keys
APVB65	Modular furniture mount for 45 function keys
APVR11	PM/C, no function keys, with case
APVR12	PM/C, no function keys, without case
APVR13	PM/C, 45 function keys, with case
APVR14	PM/C, 45 function keys, without case
APVR15	PM/C, no function keys, with case, with light pen
APVR16	PM/C, no function keys, without case, with light pen
APVR17	PM/C, 45 function keys, with case, with light pen
APVR18	PM/C, 45 function keys, without case, with light pen

9.1.4 Light Pen Option

A Light Pen and Electronics Unit may be implemented as an accessory to a keyboard to provide quick control over the position of the displayed cursor. When the pen is touched at a character position on the display screen with a small amount of pressure needed to close a pair of contacts,

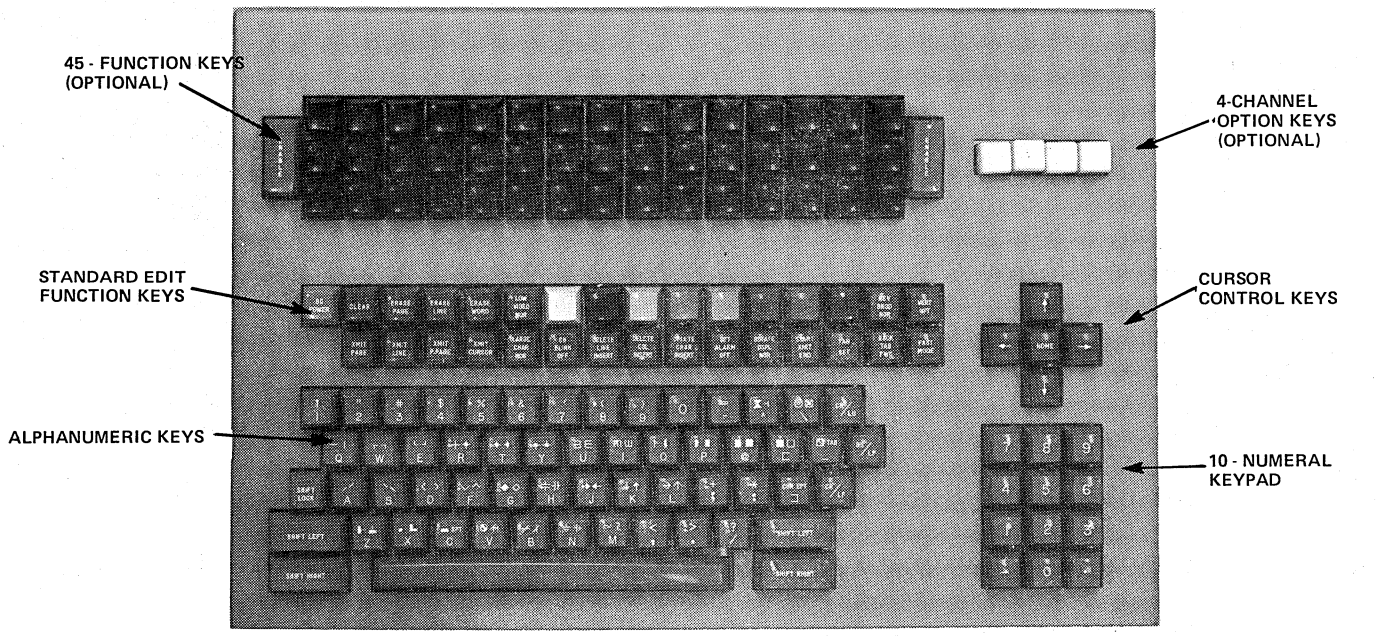


Fig. 9-3 General Purpose Keyboard

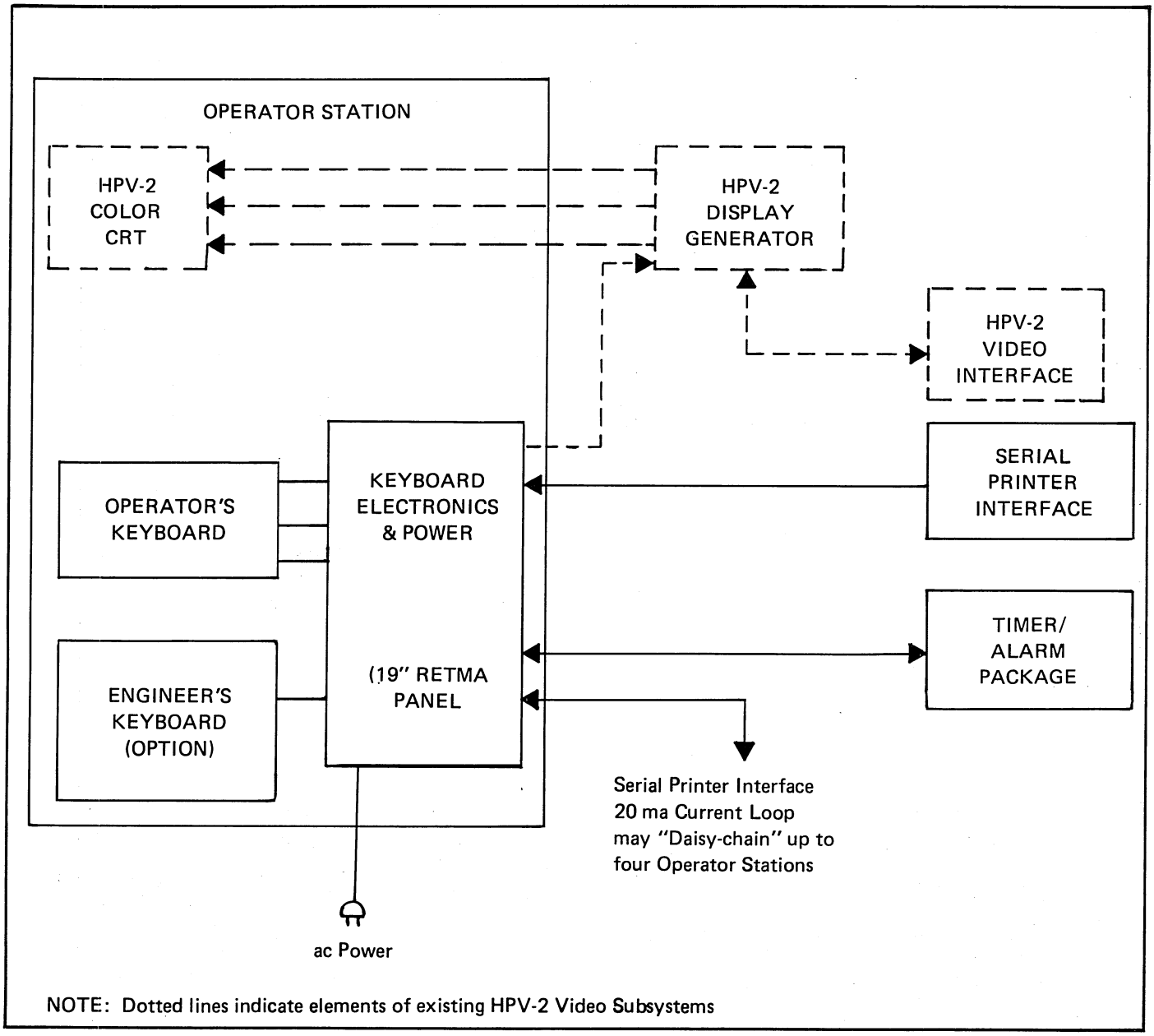
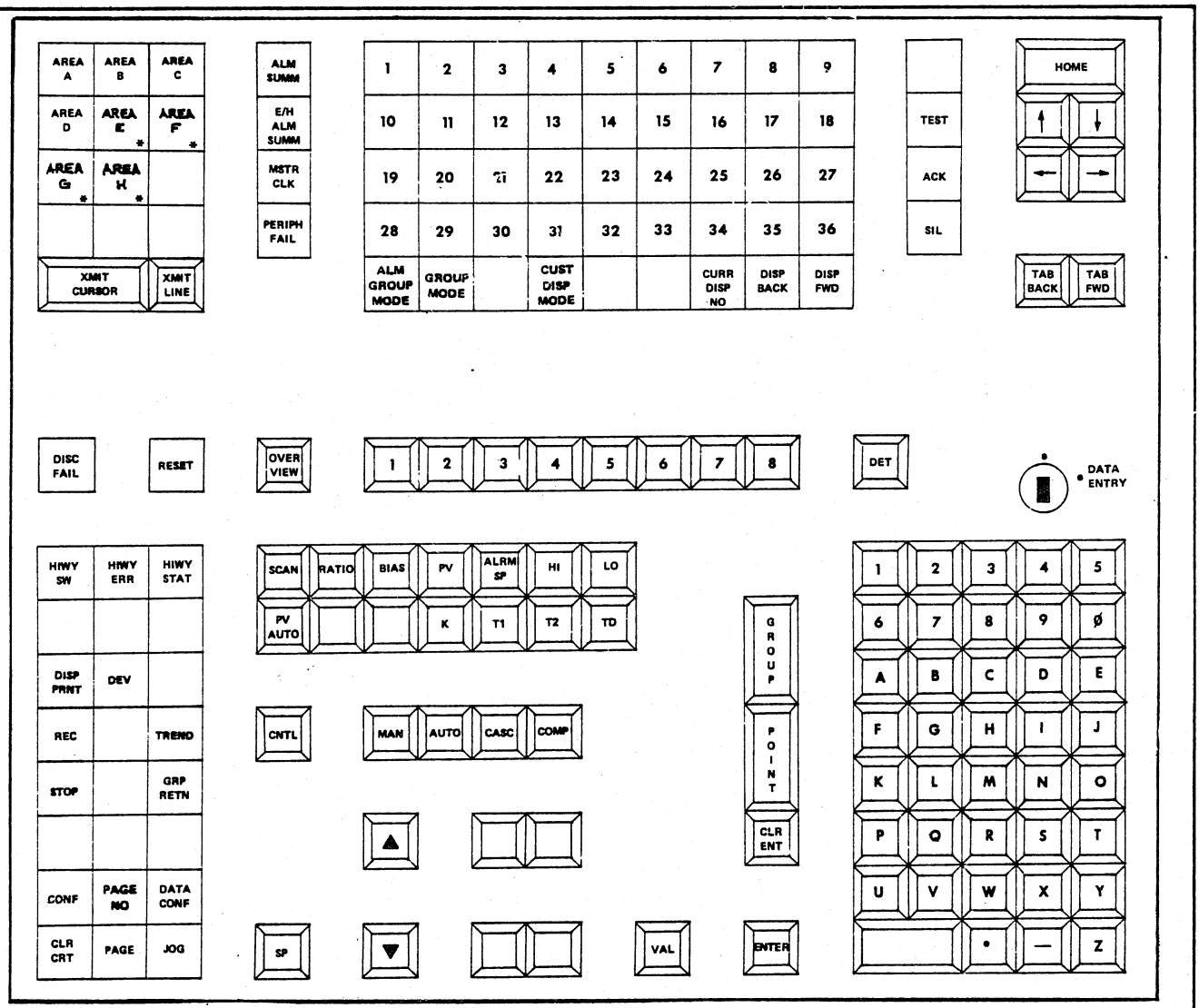
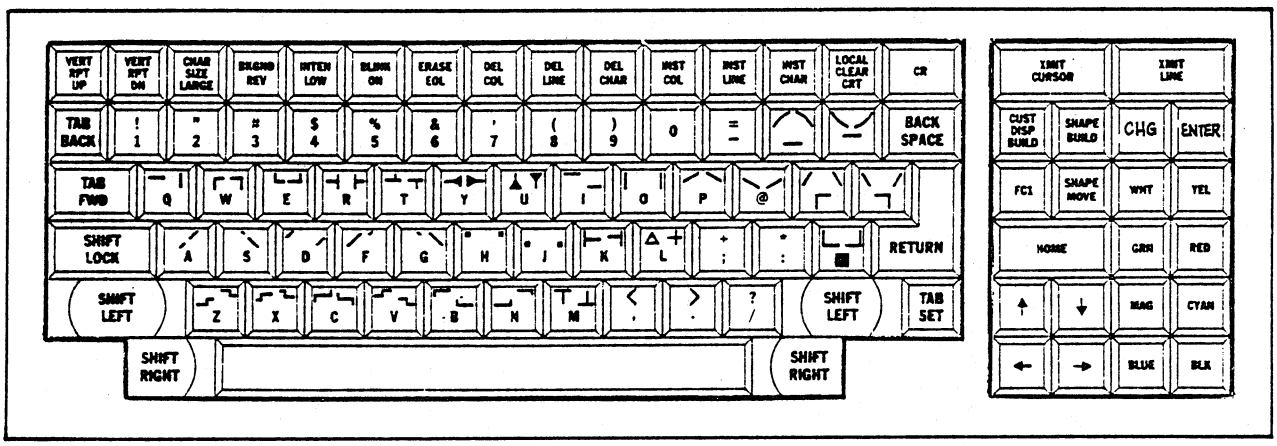


Fig. 9-4 Supervisory/Total System Keyboard Block Diagram



OPERATOR'S KEYBOARD



ENGINEER'S KEYBOARD

* Total Systems Only

Fig. 9-5 Supervisory/Total Operator's and Engineer's Keyboards

the cursor moves to that position almost immediately. When the operator pushes a button on the body of the Light Pen, a cursor coordinate message is transmitted to the computer.

9.1.5 Supervisory/Total System Keyboards

The Supervisory and Total Systems use two different keyboards. Each of these keyboards is designed for easy operation with few key strokes per function, and may be housed in modern Modular Furniture. See Fig. 9-4 and 9-5.

An Operator's Keyboard is provided with each Supervisory or Total Station. This keyboard is used by the process operator to call up a broad range of displays on a CRT and to make changes in limits, range, control constants, and configuration parameters. The keyboard has a Keylock Switch that prohibits functions reserved for the process engineer, backlit pushbuttons and status indicators, cursor controls, alphanumeric keys, and function buttons that reduce key strokes for commonly-used functions. When an operator uses the function buttons to transmit a function code to the computer, the computer software recognizes that a predetermined system function is being requested and makes the proper response.

One Engineer's Keyboard is provided with a Supervisory or Total System. Each of from one to three additional stations may be provided with an additional optional Engineer's Keyboard. These keyboards are used by the process engineer to apply the system to his process by creating unique displays and printed reports. The keyboard has a typewriter-style keyboard layout to make alphanumeric data entry more convenient.

These same keys are used to enter graphic symbols on the displays, as engraved at the key tops. Thus, tabular displays containing only letters, numbers, and punctuation may be constructed, or schematic and symbolic displays may be constructed from combinations of alphanumeric and graphic characters. The Engineer's Keyboard also features function keys that call for predetermined display and report building functions, to simplify these operations. Further, these keyboards feature editing keys (column-line-character insert/delete), color selection keys, and cursor positioning keys.

The process engineer uses the Operator's Keyboard to build the process I/O data base. It is this function that the Key Switch on the Operator's Keyboard permits when in the "enable" position.

Cable interfaces are made to the HPV-2 Display Generators, the Standard Serial Printer drive, and the 4500 Timer/Alarm Package. The Display Generator Interface transmits the key stroke code from either the Operator Keyboard or the Engineer Keyboard for normal video control. The Serial Printer Interface controls the "backlighted" keyboard functions and acknowledgement of function code reception, and sounds an alarm if the function codes are not received or if the transmit (FIFO) buffer is full. The interface to the 4500 Timer and Alarm Package provides the operator with system failure indication and an interface to the operator's RESET pushbutton for initialization of the system.

Supervisory/Total System Keyboard model numbers are:

4DP3AAOSK101	Operator's Keyboard (SUPER)
4DP3AAOSK102	Operator's Keyboard (TOTAL)
4DP3AAOEK101	Engineer's Keyboard Option

9.2 OPERATIONAL FEATURES

The computer program communicates with the display subsystem via DMA and GEN 2 instructions addressed to the Video Interface Controller on the GENIE I/O Bus. The Video Interface Controller formats and controls the blocks of information between the computer and the Video Display subsystem.

All messages from the computer to the Display Generator are compiled by the program and must start with a Start of Header (SOH) character, followed by the Channel Address, Command, Text, and end with an End of Text (ETX). A normal ending requires an ETX.

In response to a message sequence from the computer, the Display Generator transmits a sequence which starts with a Start of Message (SOM) Interrupt, followed by the SOH, Channel Address, Data, and ending with the ETX and the End of Message (EOM) Interrupt. When a response is not required by the Display Generator, only the EOM Interrupt will be transmitted.

Both the computer and the keyboard can enter display characters, color switch codes, blink codes, a Start Partial Transmit (SPT) character, and End Partial Transmit (EPT) character, and cursor control characters into a Channel Set. The computer and the keyboards have full control over the cursor and can initiate edit function such as line insertion, word insertion, line erasure, word erasure, and tabulation functions. The computer can change information on the display without disturbing the location of the visible cursor. The SPT and EPT characters define display segments to be transmitted to the computer in response to a computer Partial Page Information (PPI) message.

9.2.1 Alphanumeric Channel Set

Each Alphanumeric Channel Set provides video outputs for one color Display Monitor. The Channel Set contains the memory necessary to store a total of 4,096 15-bit data words of which 3,840 are required for a normal display picture with the remaining used for Tab Information. The Channel Sets also contain the logic for edit functions, cursor movement, responses to the computer, and the PROM Character Generator which produces the 128 display characters and symbols. Each 15-bit data word contains seven data bits, three color bits and five other bits that define the blink status, size of the character, protect, reverse color and reduced intensity.

The color Display Monitor displays alphanumeric characters on 48 lines with 80 characters per line, using the normal font, or 24 lines with 40 characters using the large font. This is equal to 3,840 normal size character positions or 960 large character positions per display. The normal alphanumeric font uses a 5 x 5 character format in a 7 x 7 matrix while the large font uses a 7 x 9 format in a 14 x 14 matrix to produce each alphanumeric or graphic character on the display.

A character entry cursor (blinking white square) appears in one of the 3,840 character positions if a keyboard is connected to the channel generating a display. If a keyboard serves more than one independent display, via the four-channel output switch option, the cursor appears only on the channel selected. Even though the cursor is not displayed, the position, at which the next character is to be entered, is stored in a cursor position register in the Channel Set. As characters are entered on the display the cursor position is automatically incremented from left to right along each line and from line to line. The cursor position may be interrogated by the computer or it may be changed by the computer, a keyboard, light pen, trackball, or a joystick, and the changed position may be transmitted to the computer as a request for some predefined action.

See Fig. 9-6 for an illustration of some of the alphanumeric/graphic display features.

9.2.2 Data Trend Channel Set

Each Data Trend Channel Set provides video outputs which display data in a format similar to that of a strip chart recorder. Up to four different tracks of data can be displayed. The analog data on each track is presented with its magnitude on the horizontal axis and time on the vertical axis.

The update rate of the display is determined by the computer and the time scale can be programmed to represent seconds, minutes, days, etc., as required by the application. Data automatically advances from top to bottom as each new data point and time line is received. The resolution of the display is 512 magnitude elements in the horizontal direction by 256 time elements in the vertical direction. Vertical amplitude (Chart) lines are displayed in green with every fifth line intensified. The amplitude scale can be varied and the spacing between amplitude lines can be any number up to 16 elements maximum.

Horizontal time lines are displayed from the left limit to the right limit for each track. Time lines automatically move with each new data point so that the time reference is always correct.

Data points are entered in any one of the four data tracks, each of which is associated with one of four colors (track 1 is white, track 2 is yellow, track 3 is cyan, and track 4 is magenta).

An offset value can be assigned for each data track. This value added to each data point provides greater flexibility in overall data track positioning. Base line and shading are used to enhance the data trends and provide a zero reference. When shading is specified, all element positions from the base line to the data points are illuminated at reduced intensity. When over and under limits are specified, the space between the limits and the data points are shaded in red when the data points exceed the limits.

The Data Trend Channel Set generates the actual data plots, time lines, and amplitude grid, while the alphanumeric notation is provided by the Alphanumeric Channel Set. The output of the Data Trend and Alphanumeric Channel Sets are "ORed" on the Data Trend and presented to the display. Colors for the alphanumeric and the data points will not mix to form a different color.

The Trend Channel Set is addressed in the same manner as the Alphanumeric Channel Set and all data points are entered like cursor coordinates are in Alphanumeric Channel Sets.

9.2.3 Video Display

The colors that appear on the color displays are produced as a result of the combination of one, two, or three of the primary additive colors on the CRT screen, as dictated by the video pulses on the three video output lines for each Channel Set. The colors and video signal combinations are:

White = Red, Green, and Blue

Yellow = Red and Green

Cyan = Green and Blue

Magenta = Blue and Red

Red

Green

Blue

When the relative intensity of the three primary colors is adjusted to produce white as perceived by the human eye, characters displayed in blue have low intensity and contrast, and the use of blue as one of the displayed colors is not generally recommended.

9.3 COMPUTER/DISPLAY GENERATOR MESSAGES

The Display Generator notifies the computer that it has information to send by placing a Transmit Interrupt word on the data lines and activating the interrupt line. The Display Generator does not transmit information or error messages unless requested to do so by the computer. The computer and the Display Generator can exchange messages containing a full page of display information, partial page of information, and the Display Generator may notify the computer of a refresh memory parity error, in code messages, partial page information messages, full page messages, and cursor information messages to the computer. The message sequences, formats and character codes are extensive and not described in detail here. They are described in detail in the Operation section of the theory publication number 4400AR94-T and HPV-2 Communications Manual, PTS-036.

9.4 ADDITIONAL FEATURES

9.4.1 Physical Characteristics

The approximate physical characteristics of the video display equipment are:

Display Generator; (rack mounted in an ASU); 222.25 mm (8.75") H x 482.6 mm (19") W x 508 mm (20") D, 35 lbs.

Display Monitors; 19" (482.6 mm) color - 482.6 mm (19") H x 444.5 mm (17.5") W x 609.6 mm (24") D, 99 lbs; 25" (635 mm) color - 558.8 mm (22") H x 609.6 mm (24") W x 609.6 mm (24") D, 130 lbs.

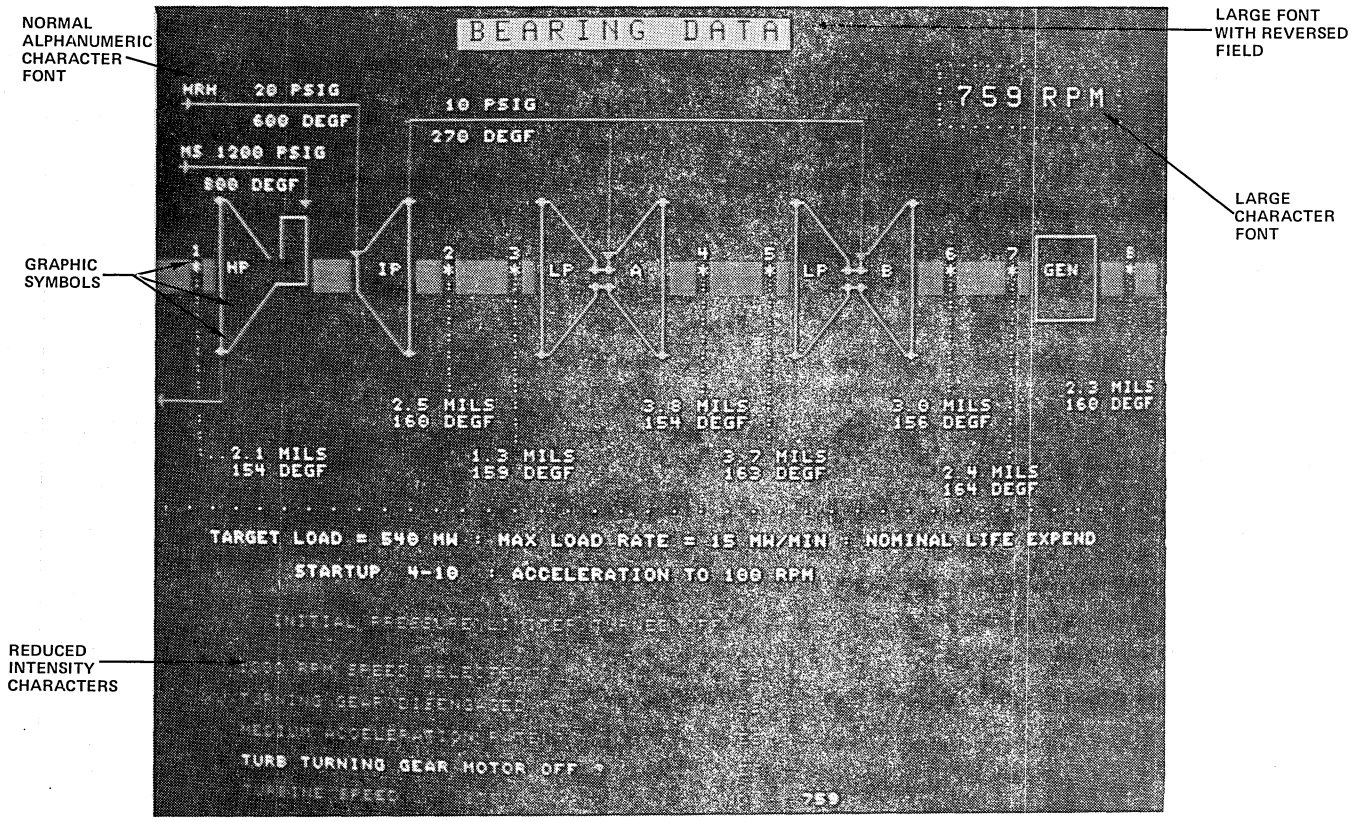


Fig. 9-6 Alphanumeric Display Features

General Purpose Keyboard; with case - 119.38 mm (4.7") H x 444.5 mm (17.5") W x 206.25 mm (8.12") D*. Flush mount - 73.66 mm (2.9") H x 444.5 mm (17.5") W x 234.95 mm (9.25") D**.

Special Keyboard (General purpose standard with 45 function keys); with case - 134.26 mm (5.3") H x 444.5 mm (17.5") W x 292.1 mm (11.5") D*. Flush mount - 73.66 mm (2.9") H x 444.5 mm (17.5") W x 302.26 mm (11.9") D**.

45-Function Key Keyboard; with case - 119.38 mm (4.7") H x 444.5 mm (17.5") W x 208.28 mm (8.2") D*. Flush mount - 63.5 mm (2.5") H x 444.5 mm (17.5") W x 234.95 mm (9.25") D**.

Supervisory/Total Operator's Keyboard; Flush mount; Lower - 10.16 mm (.40") H x 394.97 mm (15.55") W x 198.37 mm (7.81") D; Upper - 10.16 mm (.40") H x 394.97 mm (15.55") W x 103.12 mm (4.06") D.

Supervisory/Total Engineer's Keyboard; Flush mount - 9.27 mm (.365") H x 394.97 mm (15.55") W x 122.94 mm (4.84") D.

Light Pen; 19 mm (3/4") diameter x 152.4 mm (6") long, 4 ounces, 152.4 cm (5') cable.

9.4.2 Power Requirements

Display Generator; 115 Vac ±9%, 50/60 Hz, +5 Vdc - 23.5 Amps, +12 Vdc - 2.7 Amps, -12 Vdc - 1.0 Amp.

Display Monitors; color - 115 Vac ±9%, 50/60 Hz, 2.4 Amps nominal running current.

General Purpose Keyboard; 115 Vac ±9%, 50/60 Hz, approximately 60 Watts.

Supervisory/Total Keyboard - 115 Vac ±9%, 50/60 Hz, approximately 100 W.

Dc power will be supplied to the Display Generator by OEM series dc power supplies mounted on a hinged panel or from a voltage regulator on the 100 Amp/150 Amp power page. For additional details concerning the dc power supplies see the System Power section in the TDC 4500 Theory of Operation Manual.

9.4.3 Environmental Classes

The HPV-2 Display Generator is in class A, with the keyboard, monitors, and cursor control in class C. See Section 3.1 for additional environmental information.

9.4.4 Display Generator Interface

The HPV-2 Subsystem offers parallel or serial communications with the computer. The Display Generator Interface Board contains both the parallel and the serial interface circuits.

The parallel interface is an 8-bit data plus 1-bit odd parity, full-duplex, directly connected interface. All outputs are driven by open collector TTL circuits capable of driving 37 standard TTL loads in the negative direction. The parallel interface is capable of transmitting up to 600,000 bytes per second over the twisted pair leads.

The serial interface is an asynchronous data link capable of transmitting at 1800, 2400, and 9600 baud rates. The serial message word consists of 11 bits, 8 data, 1 odd parity, and 1 start and 1 stop bit.

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*1.5" of space is required behind the keyboard for power switch and cabling.

**Access and space is required for power switch and cabling at rear of keyboard.

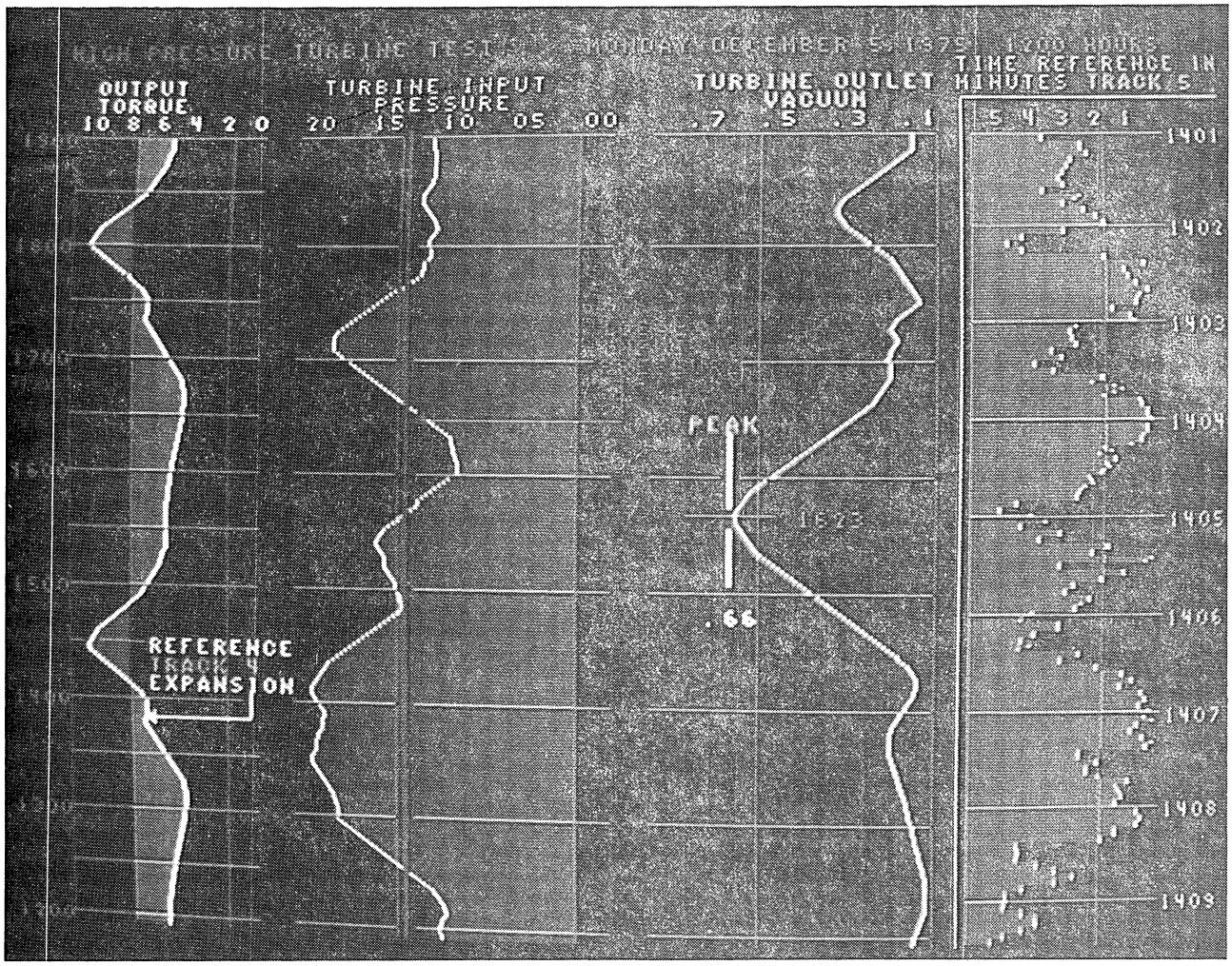


Fig. 9-7 Trend Display Features

The HPV-1 Honeywell Process Video Display System provides a reliable low-cost monochrome television-type display in a modern desk-top terminal or modular components. Up to 24 lines of 80 numbers, letters, punctuation marks, and graphic characters may be displayed.

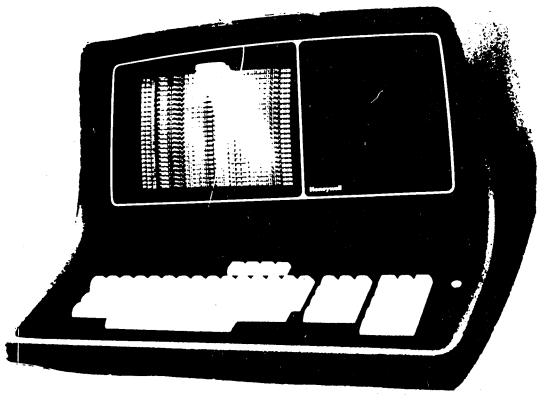


Fig. 10-1 Table-Top Terminal

HPV-1 subsystem consists of an asynchronous serial data link with the GENIE I/O Bus, a desk-top television terminal with built-in keyboard and display electronics or a 23-inch TV screen with separate display electronics and optional modular keyboard. Display information may be entered from the Central Processor or by keyboard. Data may be entered into the computer a character, line, or a page at a time. Information on the display appears as bright characters on a dark background.

10.1 OPTIONS

10.1.1 Terminal Options

HPV-1 monochrome video terminals provide half or full duplex operation and permit operation at one of five selectable baud rates from 110 to 9600 baud. Highly reliable solid state type displays are used in all cases. The 23-inch monitor is available with a yoke mount or table-top cabinet. The desk-top terminal is an attractively styled unit containing 12-inch (diagonal) display, keyboard, and Display Generator. Modular terminal components are available as separate elements suitable for user mounting or factory mounted in a 30-inch high table.

Terminal model numbers are:

- APVA2X Desk-top Terminal with self-contained 12-inch screen, keyboard, and Display Generator.

  X = 1 110 V, 60 Hz - without Function Keys

  X = 2 110 V, 60 Hz - with Function Keys

  X = 3 220 V, 50 Hz - without Function Keys

  X = 4 220 V, 50 Hz - with Function Keys

- APVA3X Modular Terminal Components

  X = 1 = Display Generator only

  X = 2, 3 = Display Generator and Keyboard - 60 Hz 115 V, with (X = 3) or without (X = 2) Function Keys

  X = 4 = Display Generator only - 50 Hz 230 V

  X = 5, 6 = Display Generator and Keyboard - 50 Hz 230 V, with (X = 6) or without (X = 5) Function Keys

- APVA5X 23" CRT

  X = 1 = Yoke Mount CRT - 60 Hz

  X = 2 = Table Mount CRT - 60 Hz

  X = 3 = Yoke Mount CRT - 50 Hz

  X = 4 = Table Mount CRT - 50 Hz

- APVA4X Modular Furniture

  X - 1, 2 = 26.8" by 30.1" by 36" (WxHxD) Table with 19" rack mount facility, with (X = 2), or without (X =1) cutout for keyboard.

10.1.2 GENIE Interface Options

A serial asynchronous GENIE I/O Controller links display and keyboard with the Central Processor. Terminal devices on the EIA RS232 interface may be up to fifty feet from the Bus Controller.

Both transmitter and receiver are contained on a single 10" x 15" (AXPV11) printed wire board.

The AXPV11 controller board connects to video equipment through a model AZAE10 fifty-foot EIA cable. Current loop and modem cables as well as other length EIA cables are available on special order.

The video Display Generator and controller may also be remotely connected using model 4400AH40 modems. The current loop (special order) permits direct connection up to 1000 feet.

10.2 OPERATIONAL FEATURES

The Display Generator uses an internal memory to store information contained on the display. Either the computer or optional keyboard may change this information. Using TIM/TOM and GEN 2 instructions, the program communicates with display electronics through the asynchronous controller.

10.2.1 Editing Controls

A blinking underscore entry marker (cursor) may be moved up, down, forward, or backwards by the operator to indicate where the next character will be entered. The cursor may be computer positioned before reading a line or page to indicate the first text character. Other editing controls are provided to erase the screen, tab, and insert/delete a line or character.

10.2.2 Operating Modes

Any of these operating modes may be selected by the operator:

- Conversational mode allows each keyboard character to be transmitted when it is depressed. In half duplex mode, the character will (if displayable) also appear on the last display line. After filling the entire line, the displayed text will move up to permit a new bottom line.

- Message mode permits an operator to display and edit any line. When the transmit key is pressed, that line containing the cursor will be transmitted to the computer.

- Page mode allows the operator to display and edit an entire screen before transmitting. When only partial screen transmission is desired, an EOT-ETX character pair may be used to specify the termination point. True Page mode is present but not supported by standard software. Instead, a Pseudo Page mode provides the same editing advantages and does so with a fraction of reserved memory space needed for true page input.

- Pseudo Page mode is a RTMOS option that functions with the terminal in the Message mode. The operator requests a full or partial page input by pushing the "." (decimal) key in the numeric keypad. RTMOS recognizes this as a request for a full or partial page input. It then finds memory space, and reads in each line until an EOT-ETX character pair terminates the input, or until the end of the page is encountered.

Mode control switches are located on the keyboard or, for modular systems without a keyboard, a similar switch is provided on the Display Generator. RTMOS input routines redefine the numeric pads's (.) key as the Page mode switch to allow more efficient use of main memory.

10.3 ADDITIONAL FEATURES

10.3.1 Tagged Fields

A field of tagged characters may be originated by computer generation of the ASCII Shift Out (SO) code or Control-N on the keyboard. The field is ended by an ASCII Shift In (SI) code or Control-0 on the keyboard. Characters entered in this manner blink. Three types of characters are used in a tagged field:

Protected Data

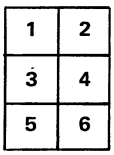
Graphic Data

Slow Blinking Data

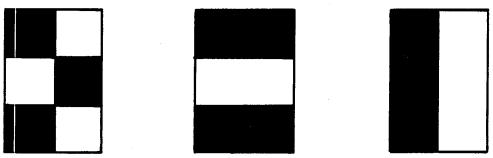
Protected data is often used to create a format. The cursor and tab will skip over protected data fields thus preventing alterations. The erase key will not erase protected data and protected data cannot be transmitted from the terminal while the Format-On state exists.

Protected data is generated during the Format-Off state by entering tagged characters as described previously. When the ASCII character "RS" or keyboard Control- ↑ is subsequently generated, the blinking tagged characters change to half intensity and become protected. The Format-Off state is commanded by an ASCII "US" character or Control- ← on the keyboard.

Graphics mode causes a tagged alphanumeric character:



Any or all of the sections are brightened according to corresponding "1" bits in the alphanumeric ASCII code. Vertical lines, horizontal lines, or patterns may be drawn in this manner:



Graphic mode is entered when the Display Generator receives an ASCII "EM" code (or Control-Y from the keyboard) and is exited upon receipt of either the Format-On or Format-Off (RS or US) code.

Slow Blinking Data. Tagged data normally blinks four times per second. Data between left and right hand brackets blinks twice per second. Protected data is at half intensity and also blinks at twice per second but graphical data does not blink. Brackets are generated on the keyboard by Shift- [(left bracket) and Shift-] (right bracket).

10.4 STANDARD SOFTWARE

10.4.1 RTMOS

The Real-Time Multiprogramming Operating System, a time proven process control program, can operate up to 32 of these asynchronous controllers. RTMOS permits the numeric pad keys 0-9 to be used in pairs so as to act as 100 function keys to request predetermined actions by the process computer system. Refer to the RTMOS Application Manual, PTS-038, for further information.

10.4.2 FILES IV

This program, working with RTMOS, has the capabilities to create, modify, resequence, print, or remove a file. It may also add or delete records from a file, merge files and/or parts of files.

10.5 COMPUTER/DISPLAY GENERATOR MESSAGES

Messages exchanged between the computer and the Display Generator consist of bit-serial ASCII characters transferred asynchronously over the EIA RS232C or current loop interface. The characters consist of "displayable" characters and control characters and there is no predefined message format. Details of the effect of the control characters and displayable characters are provided in theory publication APVA-T and the accompanying video terminal manual. Information on calls to RTMOS to transfer messages between the computer and Display Generator are provided in the RTMOS Application Manual, PTS-038. Asynchronous controller theory is described in publication AH361-T and AXPV1-T.

10.6 OTHER CHARACTERISTICS

10.6.1 Desk-Top Terminal

Screen Size:	12"
Size:	22" x 15" x 23" W x H x D
Weight:	52 pounds maximum
Power:	110 V 60 Hz, or 220 V 50 Hz, ±2%
Interface:	EIA RS232-C or 20 ma Current Loop. 110, 300, 1200, 2400, or 9600 baud.
Environmental:	Class C (see 3.1)

10.6.2 Modular Components

23" Monitor:

Size:	24" x 22" x 19" W x H x D
Weight:	99 pounds
Power:	115/230 V, 50/60 Hz, 95 Watts
Environmental:	Class C (see 3.1)

Display Generator:

Mounting:	19" Rack
Size:	19" x 7" x 12" W x H x D
Weight:	28 pounds
Environmental:	Same as desk-top model
Interface:	Same as desk-top model
Power:	115 V, 60 Hz; 230 V, 50 Hz

Keyboard:

Size:	20" x 4" x 8" W x H x D
Environmental:	Class C (see 3.1)

Table (cabinet for modular components):

Size:	27" x 30" x 36" W x H x D

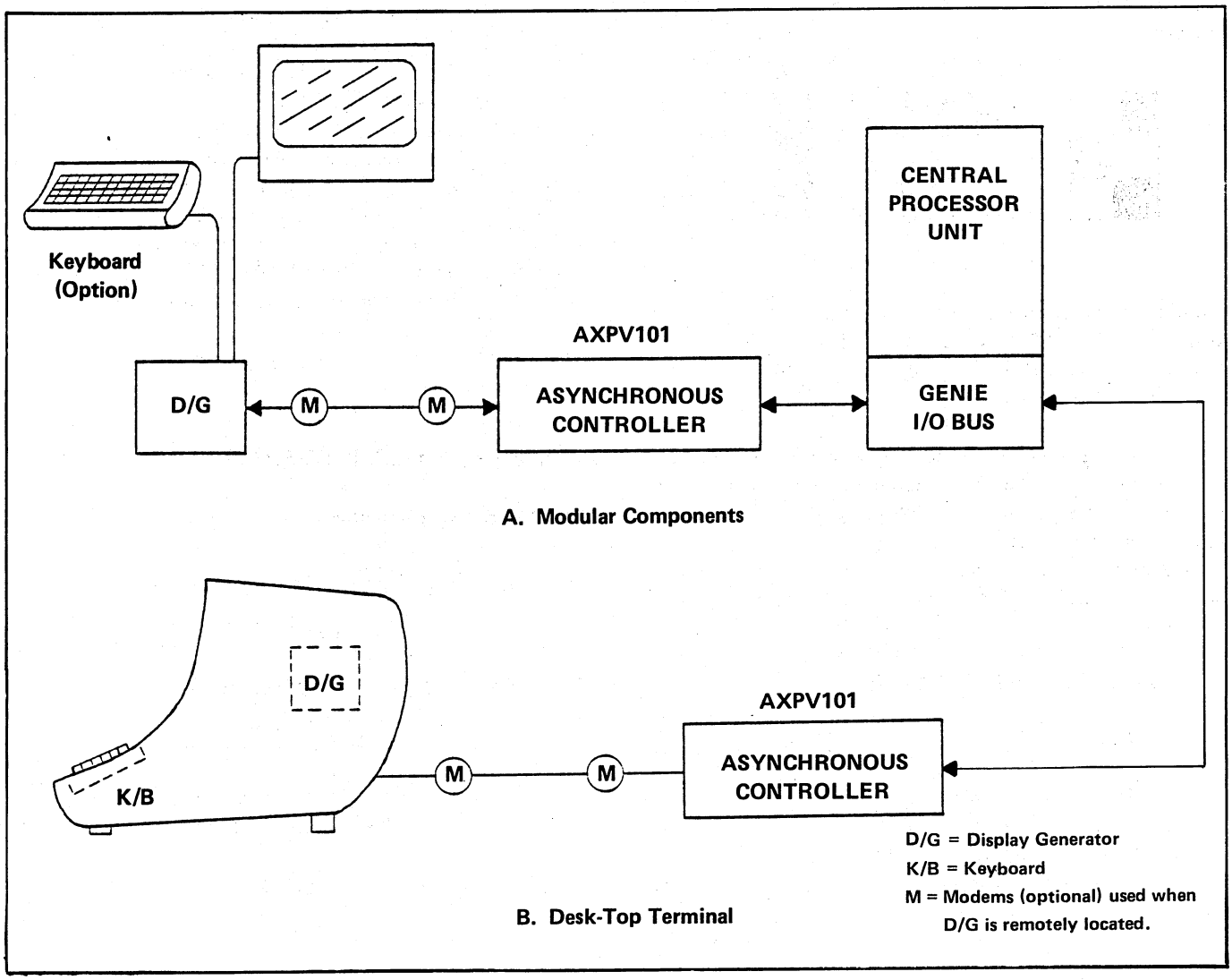


Fig. 10-2 HPV-1 Configurations

DIGITAL PROCESS INTERFACE SUBSYSTEM

The Digital Process Interface subsystem is one of the process control computer system's primary interfaces with the actual control and sensor elements within the process. The APID1 Series Digital Process Interface (DPI) subsystem is designed for the following primary attributes: Flexibility and modularity, communication with process areas located up to 500 feet (up to 2500' on special order) from the computer site over simple interconnecting cables, and an easy interface with a very large variety of process controls and sensors. Each DPI subsystem can interface with up to 2048 input or output points.

As its name implies, the Digital Process Interface subsystem provides the computer system's digital input and output interface with the process, however, the DPI subsystem also provides analog voltage or current outputs. The DPI Subsystem also serves as the system's interface to special Process Operator's Consoles.

This section of the 4500 General Description provides a functional description of the APID1 DPI subsystem and its options. System digital inputs may also come through the Data Hiway Interface module described in section 13. Application information pertaining to program control of the interface modules (typically through RTMOS) is provided in Appendix B.

11.1 FUNCTIONAL DESCRIPTION

As indicated on Fig. 11-1, the DPI subsystem consists of a Local Controller on the GENIE I/O Bus and one or more Termination Assemblies. The Local Controller serves primarily as a serial communications interface with the Termination Assemblies (TA's) which contain the majority of the DPI subsystem's control logic. The running program furnishes instructions to the Local Controller that dictate the operating mode for subsequent information transfers between the Central Processor and the user's process circuitry connected to the Termination Assemblies. The mode instructions specify the direction in which information is to be transferred, and arm or disarm the DPI subsystem API's.

Input transfers provide the status of the process or Operator's Console inputs to the DPI subsystem to the program. Output transfers convert the data provided to contact closures, analog output signals, digital displays, etc. These transfers involve specific termination assemblies and interface modules which must be addressed from the Local Controller using information supplied by the program. Addressing is random - an address is provided by the program for each transfer. API's generated by the DPI subsystem notify the program of controller ready conditions and/or changes in process digital input status.

The Local Controller's interface with the Central Processor is the GENIE I/O Bus. Instructions issued to it direct the input and output transfers between the controller and the DPI modules that interface the actual customer circuits and the Operator's Consoles, and those transfers take place on one or two radials consisting of cables with only eight wires. Communication between the Local Controller and the interface modules is buffered and directed by control boards that plug into each Termination Assembly. Each TA also contains a special plug-in terminator board that provides additional I/O module control suited to the specific configuration of the assembly.

11.1.1 Radial Port Configuration

The Local Controller has two serial communications ports, both of which are capable of communicating with Termination Assemblies up to 2500 cable feet away. Cables over 500' long are available only on special order (RDO). The Local Controller can communicate with up to 16 TA's in any configuration on the radials that can be supported by the serial bit rate selected for communications between the Local Controller and the TA's. Where the length of either radial is more than 500 feet, the lower of two serial bit rates (455 kHz) is selected. Where each of the radials is 500 cable feet or less in length, the higher serial bit rate (909 kHz) is selected. All TA's that are more than 500 cable feet from the Local Controller must be clustered together, with minimal cable runs between each such TA. TA's may be inserted into the cable lines with long runs between the TA's only when the total radial length is 500 feet or less. Fig. 11-1 shows two examples of radial port configurations. Where more than two radials are needed to serve additional remote process areas, additional FF501 Local Controllers may be implemented.

11.1.2 Termination Assemblies and Interface Modules

Up to 16 Termination Assemblies can be addressed by the Local Controller and each TA is capable of accommodating 16 input/output process interface modules. The total number of input or output points assigned to each module is a function of its type. For example, TA's housing all input signal conditioning modules are capable of interfacing

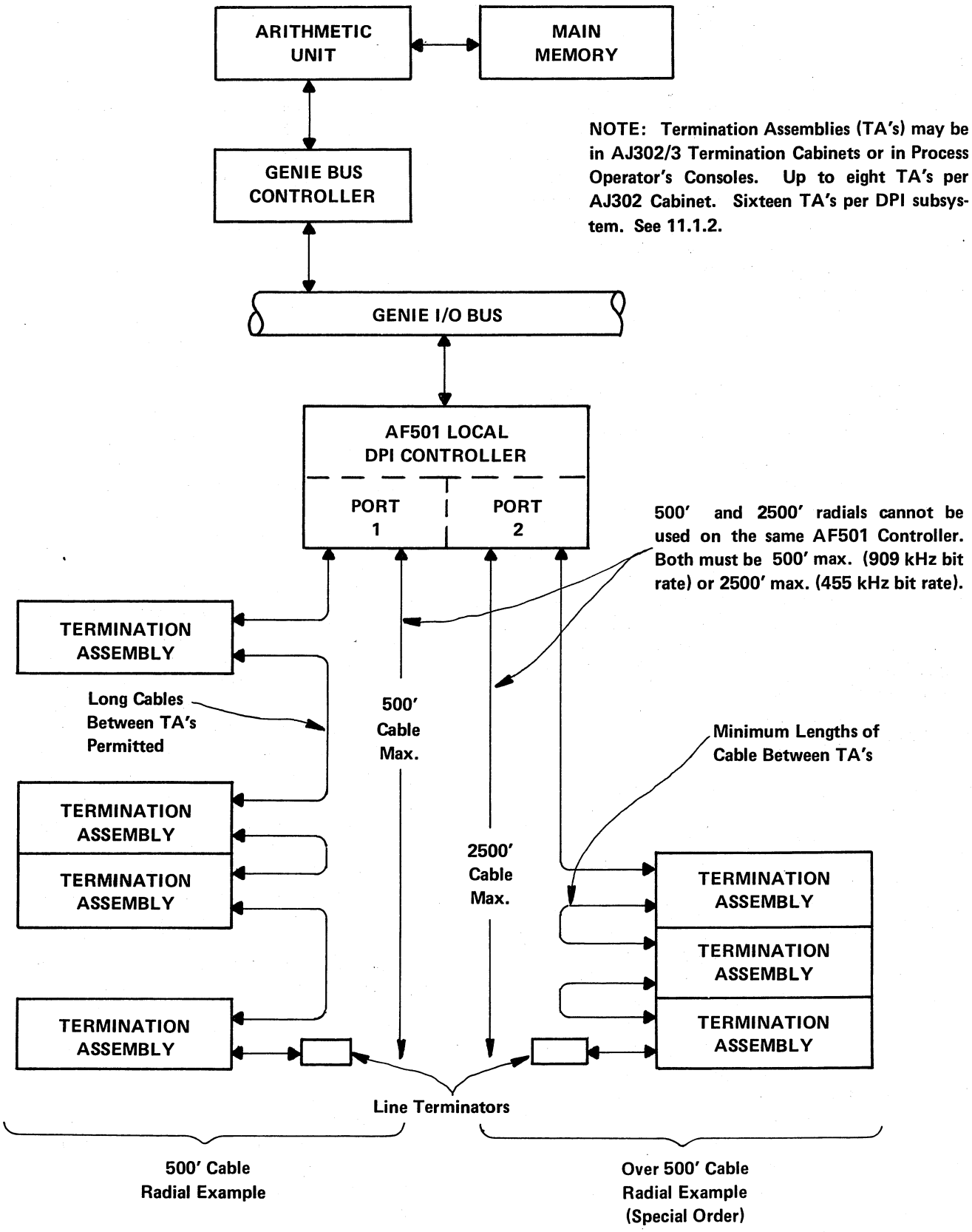


Fig. 11-1 Digital Process Interface Subsystem

128 input points (16 modules x 8 points). By comparison, TA's housing only output modules with form C contact outputs can interface only 64 output points (16 modules x 4 points). Although the maximum point capacity of the DPI subsystem is 2048 points, its applied capacity is a function of the mixture of interface modules used.

Four different TA panel arrangements are available. These arrangements are based upon the number and type of termination panels used in conjunction with the TA's (see 11.2.5). The four arrangements, their resultant maximum connection capability on a per cabinet basis, and the panel configurations necessary to achieve the arrangements are as follows:

Density Arrangements	TA's per Cab.	No. and Type of Panels per TA	Connections per Panel	Max. per Cab.
Lo	2	2 (lo)	64	256
Med	4	1 (med)	128	512
Hi	8	1 (med)	128	1024
125 V	2	1 (med)	128	256

Plug-in interface modules for input circuits can be selected according to signal level, isolation needs, filter requirements and change detect capability. Standard signal levels currently handled are 5 V (TTL), 28 V, 48 V, and 125 V. These inputs can be powered by customer supplies or by supplies provided with the equipment that mount in the termination cabinets. Point and block circuit isolation are available to permit separation of individual circuits or 8-circuit groups when customer and Honeywell supplies are intermixed. Several filter time constants are available on the input modules to reject noise transients in the circuits. Change detect input modules are available to provide automatic notification to the computer when there has been a change in the input circuit's status.

Plug-in interface modules for output circuits can be selected from momentary, latching, or confirmed output options, or from the analog output option. Both the momentary and latching outputs offer mercury-wetted relays that are available in 100 VA and 250 VA contact ratings. The momentary outputs have pin-select options on the circuit boards that permit selection of pulse periods ranging from 5 ms to 1 second. The confirmed output option provides security when selecting output circuits by permitting the computer to read back and confirm the addressed module's selection information before energizing the relay to close or open the circuit. Analog current output modules can be selected in 10-bit resolution current ranges of 0 to 5, 1 to 5, 0 to 20, and 4 to 20 milliamp ranges. Analog output modules are also available in 10-bit or 12-bit voltage versions. The 10-bit voltage output can be pin selected for unipolar 0 V or 10 V, or for one of the bipolar ($\pm$5 V or $\pm$10 V) ranges. The 12-bit voltage output is available in a bipolar $\pm$10 V range.

Display driver output boards are available at 12 V and 28 V to interface consoles or other equipment with indicators.

11.1.3 Transfer Rates

Data, commands, and status information are exchanged between the Local Controller and the Central Processor as 24-bit words, transferred through the execution of GEN 2 instructions addressed to the Local Controller (7.7 µs execution time). The overall operating speed of the subsystem depends on the serial bit transfer rate on the radial ports (909 kHz up to 500' and 455 kHz over 500') and the time required for RTMOS to initiate and process the transfers. The time required to transfer 24 bits of data at the higher bit rate (including software overhead) is approximately 500 µs and the time required to acquire change detect or sequence of events interrupt status is approximately 125 µs.

11.2 DPI SUBSYSTEM OPTIONS

Model numbers for the DPI options are provided in the following paragraphs. The TDC 4500 Configuration Guide provides additional information. See 11.2 for descriptions of the interface modules.

11.2.1 Input Modules

F5102 TTL, 0.1 µs filter

F5104 TTL, 100 µs filter, with change detect

F51xy 28 V/48 V Inputs (8 ckts./board)

x =	1	Non-isolated, 28 V
	2	Non-isolated, 48 V
	3	Special request (ac inputs)
	4	Block isolated, 28 V
	5	Point isolated, 28 V
	6	Block isolated, 48 V
	7	Point isolated, 48 V

y = 0 .1 ms filter, if non-isolated;
1 ms filter, if point or block isolated
(see x above)

1 1 ms filter, if non-isolated;
4 ms filter, if point or block isolated

2 22 ms filter

3 Change detect and filter
(.1 ms filter if non-isolated; 1 ms if isolated)

4 Change detect and filter
(1 ms filter if non-isolated; 4 ms if isolated)

5 Change detect and 22 ms filter

F53xy 125 V Inputs (8 ckts./condition and buffer board)

x = 1 Block isolation

2 Point isolation

y = 0 .1 ms filter

1 1 ms filter

2 22 ms filter

3 .1 ms filter, bi-polar change detect

4 1 ms filter, bi-polar change detect

5 22 ms filter, bi-polar change detect

6 1 ms filter, pin-selected change detect

7 4 ms filter, pin-selected change detect

8 22 ms filter, pin-selected change detect

11.2.2 Output Modules

F50x Mercury-wetted Contact Outputs

x = 1 100 VA, Form "A" latching
2 100 VA, Form "A" momentary
} 8 ckts./board

3 250 VA, Form "D" latching
4 250 VA, Form "D" momentary
5 100 VA, Form "C" confirmed (pin-select latch or momentary)
} 4 ckts./board

F5020 Solid State Latching Outputs (8 ckts./board)
50 V max.; 500 ma max.

F505x D/A Converter, Current Outputs
(2 outputs/board)

x = 0 0 - 5 ma range

1 1 - 5 ma range

2 0 - 20 ma range

3 4 - 20 ma range

F5060 D/A Voltage Output with Pin-selectable Range
(2/board)

F508 Programmed Pulse Train Generator
(Pulse Train or Timed Output)

11.2.3 Operator's Console Modules

F52x

x = 01 Digital Display Drive (28 V)

02 Digital Display Drive (12 V)

53 Keyboard Encoder

54 Console Lamp Driver

55 Lamp Driver

11.2.4 Power Supplies

Power supplies for the subsystem are as follows:

COMMON SUPPLIES (Logic and input/output)

L131 5 V Logic, 30 Amp

L132 5 V Logic, 60 Amp

L321 28 V, 2.5 Amp for relay output or for input circuits

OUTPUT ONLY

L381 12 V, 5 Amp relay supply

L382 12 V, 10 Amp relay supply

L421 ±15 V, 2 Amp analog outputs

INPUT ONLY

L311 48 V, 2.5 Amp for input circuits

L312 48 V, 5.0 Amp for input circuits

L313 48 V, 2.5 Amp for isolated inputs

L314 48 V, 6.0 Amp for isolated inputs

L322 28 V, 2.5 Amp for isolated digital inputs

L331 125 V, (60 Hz ac powered) for input circuits

L332 125 V, (50 Hz ac powered) for input circuits

L372 28 V, 6.0 Amp for isolated digital inputs

11.2.5 Termination Assemblies

F341 High Density, 128 points, terminal connections to process.

F343 High Density, 128 points, cable connections to process.

F342 Medium Density, 128 points, uses one K202 Termination Panel for terminal connections to process.

F342 Low Density, 128 points, uses two K201 Termination Panels for terminal connections to process.

F344 125 V Input TA, 128 points, uses one K203 Termination Panel for terminal connections to process.

11.2.6 Terminator Modules

Plug-in terminator modules are available in four versions, three of which contain combinations of change detect interrupt and/or momentary output timing circuitry. The fourth is a standard terminator used for assemblies that contain neither change detect inputs or momentary outputs. Terminator modules and their applications are as follows:

- F361 Terminator Module

  Used when assembly does not contain interrupt-generating change detect input or momentary output interface module.

- F362 Terminator Module (Oscillator)

  Provides pin selection of three clock frequencies from six possible (1 or 2 μs or .5, 1, 2, or 4 ms) frequencies to use in timing momentary output periods.

- F363 Terminator Module (Interrupt Control and Oscillator)

  Provides the same pin-selectable clocks for momentary output timing mentioned for F362 and includes circuitry for providing interrupt status to the controller for assembly.

- F364 Terminator (Sequence of Events)

  Special purpose terminator module used only when the assembly contains all change detect input modules. When used, this module provides status to the controller for the specific module having a circuit status change, thereby creating a simpler and faster method for the processor to acquire the interrupt information than with the Interrupt Control terminator.

11.2.7 Termination Cabinets

Termination Cabinet AJ302 is a Digital I/O cabinet while AJ303 may be shared by Digital I/O TA's and Analog Input TA's (see 11.1.2 and 12.2.1). The AJ302 cabinet may incorporate an FL511 Power Surge Limiter (see 3.2.1).

11.3 PROCESS INTERFACE MODULES

11.3.1 Input Modules

Standard input interface modules are basically selected to meet filter and change detect requirements, and to operate at the voltage levels of the circuits they interface. Basic operating levels for the input modules are 5 V (TTL), 28 V, 48 V and 125 V. Other selection criteria involve circuit isolation and change detection requirements.

11.3.1.1 Isolated Inputs

All non-isolated inputs share the same circuit common, but isolated inputs can be used to separate individual (point) circuits or groups (blocks) of circuits from other power supply references. Modules designed for non-isolated inputs can be selected from 100 μs, 1 ms, or 22 ms filter constants. (The filter constant period reflects the approximate inherent circuit delay to an input signal.) Filter constants of 1 ms, 4 ms, or 22 ms are available for point and group isolated input modules. Refer to Fig. 11-2 for typical examples of isolated and non-isolated input configurations.

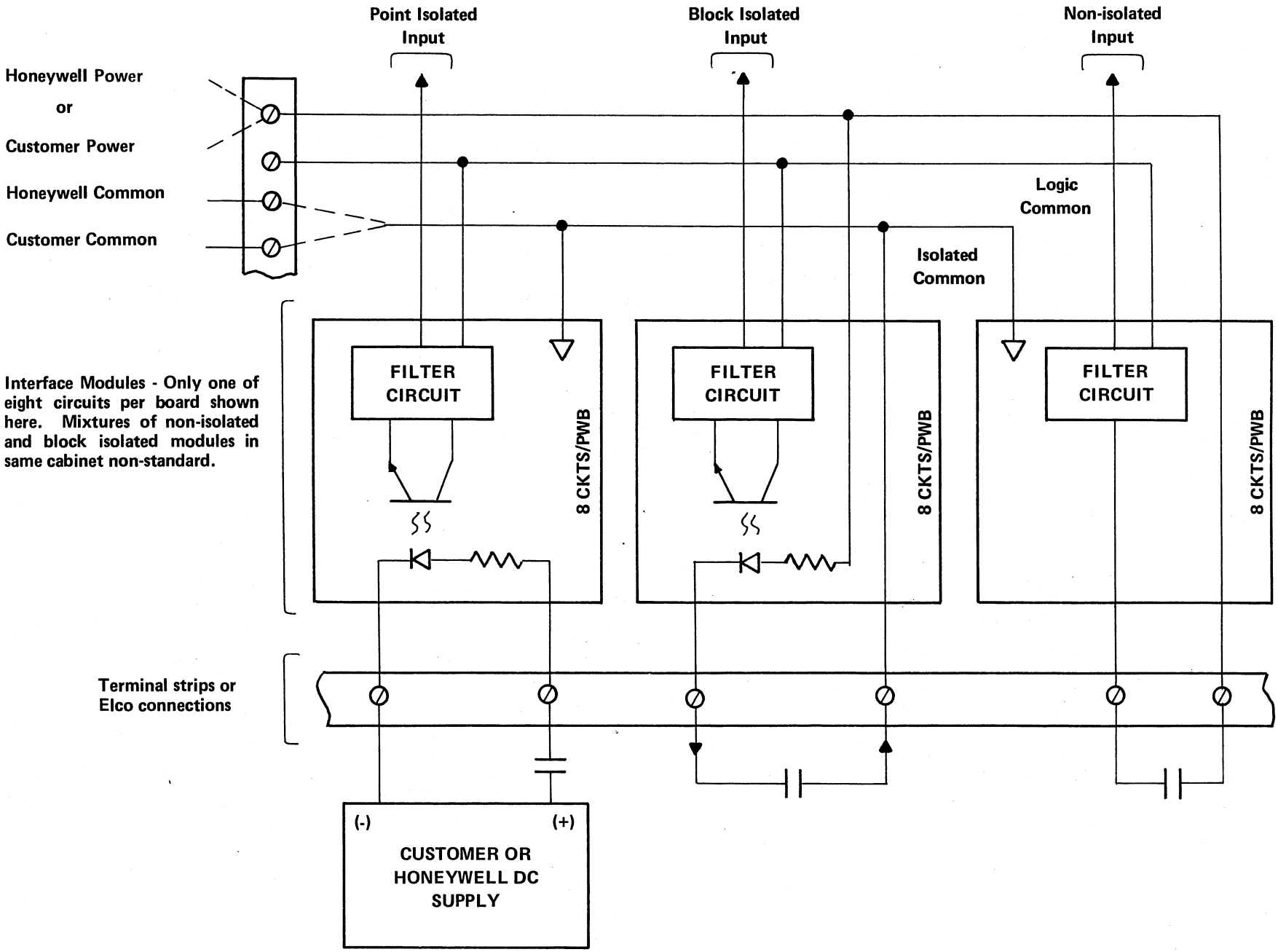


Fig. 11-2 Isolated and Non-isolated 28 V and 48 V Digital Inputs

11.3.1.2 Change Detect Inputs

Change detect interface modules can be selected from bipolar or pin-selectable versions.

The bipolar version provides interrupt notification to the processor when the input circuit status changes in either direction. The pin-selectable version permits pin selection to provide interrupt notification in the same manner as the bipolar, or to only occur with a specific change of signal direction.

11.3.1.3 125 V Inputs

As indicated by Fig. 11-3, 125 V inputs require an isolated buffer module in addition to the regular input module used for the other signal levels. These additional modules are plugged into an extra row of card slots available on the 125 V Termination Assemblies. The isolated buffer modules are available in either point or block isolated versions.

11.3.1.4 Terminator Modules

Each Termination Assembly requires a terminator module suited to the type of interface modules used in the assembly. Assemblies having no input change detect circuitry nor momentary outputs can utilize the F3601 Terminator module. The F3603 Interrupt Control Terminator module is intended for assemblies that include change detect circuitry; it also contains oscillator circuitry to enable momentary output modules to be used on the assembly. The F3604 Sequence of Events Terminator module is a special purpose terminator that can only be used if the entire assembly is dedicated to change detect input modules.

11.3.2 Output Modules

Output modules are available in version to provide contact closure, analog signal generation lamp driver (and keyboard input), programmed pulse/timed output, or display drive. Contact closure versions are selected according to contact rating (100 or 250 VA, mercury-wetted) and latching momentary requirements. Analog generator versions are selected by signal range and voltage/current signal sources. Analog voltage outputs are available in pin-selectable ranges of 0 to 10 V, +10 V to -10 V, or +5 V to -5 V. Current ranges for analog outputs are 0 to 5 mA, 1 to 5 mA, 0 to 20 mA, and 4 to 20 mA. Both voltage and current versions provide 10-bit resolution of the output signal. Display drive modules are available in versions of 12 V or 28 V operation.

11.3.2.1 Latching/Momentary Contact Outputs

Latching contact outputs require computer instructions to drop out or to energize the relay. Momentary output modules supply contact closures when instructed by the computer and then automatically drop out after a pin-selected time period. Examples of typical relay output circuits are provided by Fig. 11-4. The time period is established by a combination of clock pin selections at the assembly's termination module and clock and count pin selections at the specific momentary output module. Three basic clock periods can be pin selected from the termination module, at periods of 1 or 2 μs, .5 or 1 ms, and 2 or 4 ms. The three selected clocks are distributed to the output modules on the assembly, which are then pin selected to use one of the three clock periods for its module's counter. The counter can be pin selected to any of 256 counts. The minimum resultant momentary closure period is a function of the type of relay used: 3 ms for 100 VA relays and 5 ms for 250 VA relays. The maximum period is achieved using the 4 ms clock extended to 256 counts - equal to 1.024 seconds, plus 3 or 5 milliseconds for relay dropout.

11.3.2.2 Confirmed Outputs

The confirmed output modules are multi-purpose, containing four Form "C" relay contact outputs. These outputs can be configured as simply Form "C" latching outputs or they can be pin-selected to operate as either momentary or latching confirmed outputs. Hardware confirmation of the relay selection is primarily accomplished by a hardware comparison of the least significant four bits of the eight bits sent to the board for relay selection. Any non-comparison results in a Device Unavailable error.

The four most significant bits of the output data transfer to a confirmed output module provides selection information for the module's four relays. Final enabling of the selected relay(s) is not accomplished until the operating system sends a specific Z-bit configuration to confirm correct selection. The operating system can provide confirmation of the selection prior to enable by checking for an error following the data transmission and/or it can read back the data field from the module.

A confirmed output pin-select option provides sequential operation for groups of up to 16 confirmed output modules. The grouping is determined by special system wiring to interconnect momentary version confirmed output modules. Once interconnected by the wiring and selected for sequential operation by pin select, the selection, by program, of any one module in the group inhibits access to any other in the same group until the selected module has

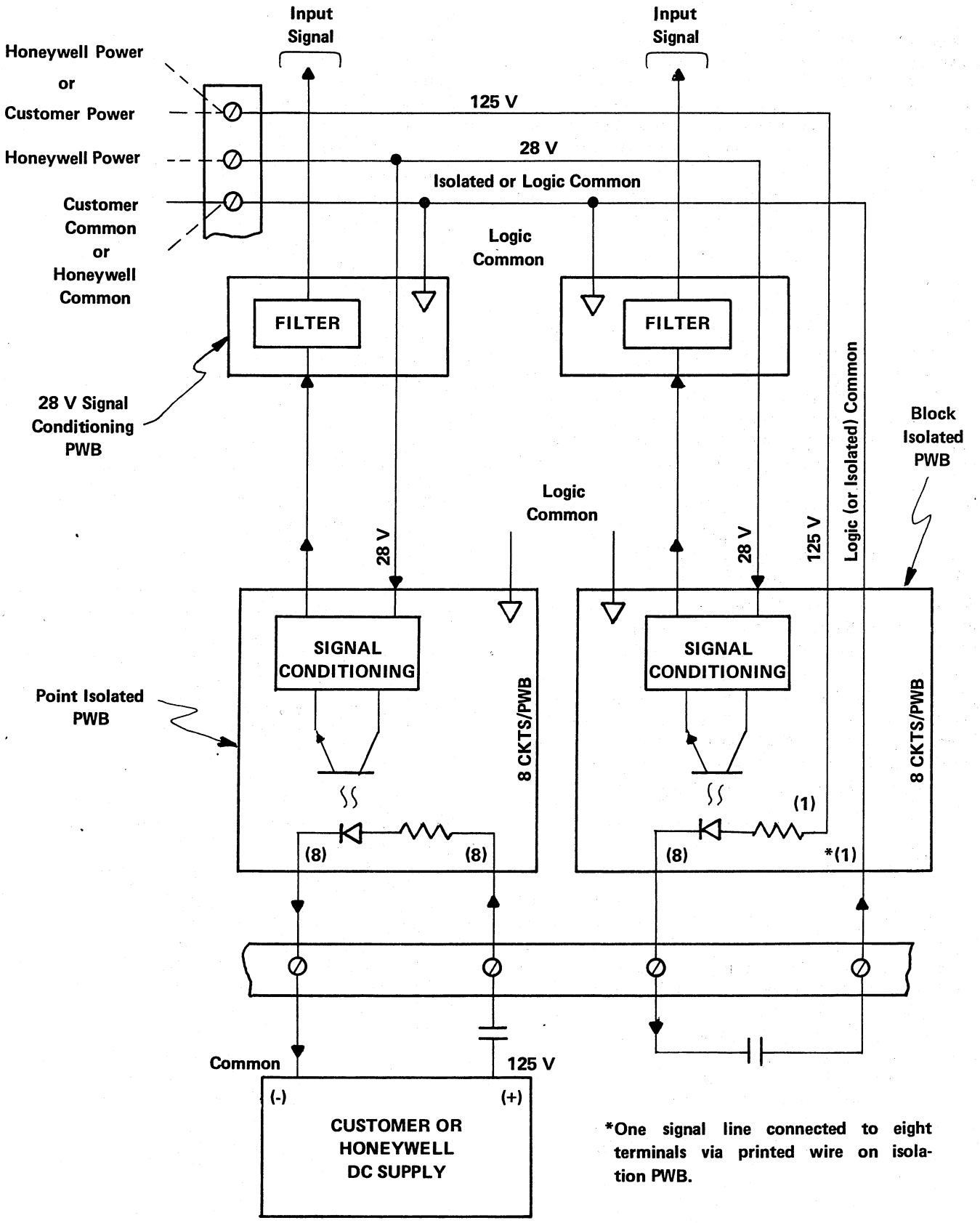


Fig. 11-3 125 V Block or Point Isolated Inputs

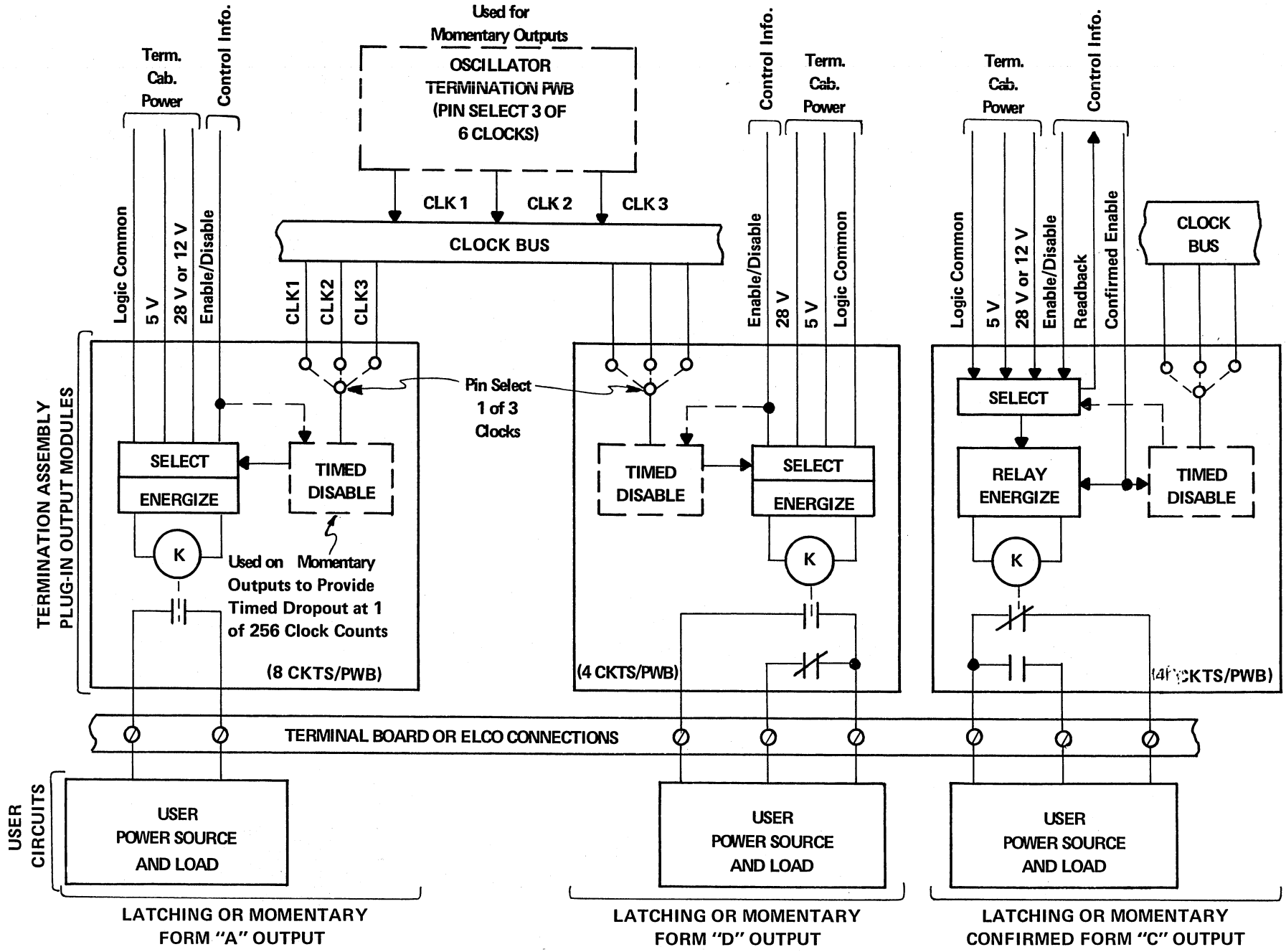


Fig. 11-4 Latching and Momentary Relay Outputs

completed its operation. Any attempt to access another confirmed momentary output module in the group while one is in operation results in a device unavailable indication.

11.3.2.3 Analog Outputs

Analog output modules are available in two voltage output versions and one current output version. One of the two voltage output versions provides 10-bit resolution for either of its two circuits in pin-select ranges of ±5 V, ±10 V, or 0 V to 10 V. The other voltage output version provides 12-bit resolution for a single analog output signal in a ±10 V range.

Current output versions provide 10-bit resolution analog output signals in ranges of 0-5 mA, 0-20 mA, 1-5 mA, or 4-20 mA.

11.3.2.4 Programmed Pulse Train Generator

The programmed pulse train generator module provides either a pulse train or timed output, as determined by pin selection at the module. The pulse train count or timed output period, as applicable, is selectable by program via an output count to the module. The module includes a read capability to indicate the timed output relay status, a time-out condition, and an output-in-progress indication.

11.3.2.5 Terminators

The standard F3601 Terminator module can be used for latching contact outputs, including the latching version of the confirmed outputs. It can also be used for analog outputs or display drivers. Momentary outputs, including the momentary version of confirmed outputs and pulse or timed outputs, require either the F3602 Oscillator or the F3603 Interrupt Control (with oscillator) terminators. When momentary confirmed outputs are used, Clock 3 from the terminator module must be set to 4 ms.

11.3.3 Operator's Console Modules

Special process operators console typically have built-in TA's which utilize the following modules.

11.3.3.1 Lamp Drivers

The PX3650ILDA1 Lamp Driver module permits selective turn-on, turn-off, or flash of any one lamp driver circuits, or up to eight at a time from the module's 16 lamp drive circuits.

11.3.3.2 Console Lamp Drivers

The console lamp driver module can be pin selected to provide a 4 x 4 sink/source matrix selection of up to 16 lamp circuits, or it can be pin selected to provide sink for selection of up to 8 lamp circuits. The circuits can be turned on or off in response to an output pattern. The modules can also be directed to transfer their status back to the AU without the circuits being affected, or the module can be directed to unconditionally clear all circuit selections after transfer of the circuit status.

11.3.3.3 Digital Display Drivers

The digital display driver module provides a one of twelve (4 source/3 sink) display select for either of two display circuits. Each circuit can also be cleared of its display.

11.3.3.4 Keyboard Encoder

The keyboard encoder module interfaces the digital process interface subsystem through the input portion of the console lamp driver module described in 11.3.3.2. Its function is to convert keyboard switch selections into codes to be held in and read from the console lamp driver module. Two different code modes can be pin selected at the module, and each mode accommodates two inputs. One mode, referred to as "X", provides a three-bit, one-of-seven binary code and a five-bit, one-of-23 code. The other code, referred to as "Y", provides two four-bit, one-of-15 binary codes.

11.4 DPI SUBSYSTEM OPERATING SEQUENCE

It is convenient to think of the operating sequence as consisting of two separate functions: (1) The continuous scanning of all digital process interfaces that generate interrupts when attention is needed from the program, and the servicing of those interrupts; and (2) the exchange of commands, data, and status information between the program and the digital process interfaces. Since the second function is accomplished through the execution of a sequence of GEN 2 instructions, this subsystem does not use data exchange API's nor the TIM/TOM feature. The Local Controller uses one GENIE Bus device address.

11.4.1 Interrupt Scanning

Termination Assemblies and process operator's consoles containing digital process interface modules (PWB's)

capable of generating interrupts contain either an F363 Change Detect Terminator module or an F364 Sequence of Events Terminator module (11.2.6). Such Termination Assemblies or process operator's consoles are polled by the local DPI controller on the GENIE I/O Bus in a sequence that is interrupted only while waiting for the program to acknowledge an interrupt. Such TA's or consoles must be assigned sequential addresses beginning with 00_8 (X'0'), and continuing as needed through 17_8 (X'F'). Once all interrupting TA's or consoles are assigned sequential addresses, the remaining addresses are available for non-interrupting TA's or consoles. The TA addresses are assigned by jumper pins on a printed wire board.

When a TA or console with an interrupt request is encountered, scanning stops until the program has executed an IN S' = 1 instruction (11.4.3) to acknowledge the interrupt and accept the interrupt status word. Scanning then resumes, either through the remaining TA's or consoles, or with the first one at address 00_8, as selected by a jumper pin in the TA.

The Local Controller generates two interrupts: The type 0 API is generated when the scanner finds a TA or console requesting an interrupt and the interrupt status word has no error bits set. The program responds with an IN S' = 1 instruction (11.4.3). The type 1 API is generated when an error bit sets in the interrupt status word. The program normally responds to this interrupt with an IN S' = 2.

The DPI modules in the TA's are slected by an option pin to generate either class 1 interrupts or class 2 interrupts. Class 1 interrupts provide status information that indicates only which half of the addressable DPI modules in the TA or console has an interrupt pending. Class 2 interrupts provide status information that indicates which one of the possible 16 individual DPI modules is requesting an interrupt.

An optional method for the handling of sequence-of-events interrupts requires the use of a third DPI subsystem interrupt that is generated by the program issuing a GEN 2 instruction to an FEI11 API Buffer on the GENIE I/O Bus, after it has acquired the sequence-of-events interrupt status information. Thus, several sequence-of-events status words can be acquired by the program before it allows servicing of the third API and begins to process the sequence-of-events information. For additional information, refer to the "Local/Remote Digital I/O Software" heading in PTS-003, the RTMOS Application Manual.

11.4.2 Command, Data, and Status Exchanges

The program initiates a DPI subsystem transfer by issuing a command word to the Local Controller with an OPR instruction. This command word specifies the major function to take place, and if required, also provides "Z" bits that specify a subfunction of the addressed DPI module. It also contains the address of a Termination Assembly and a DPI module in that assembly. It may contain an output data byte. The Local Controller goes busy upon receipt of the OPR instruction, transmits the command information to the TA and awaits its response. When it responds, the Local Controller goes not busy.

If the command word specifies a read operation, the program may then execute IN S' = 0 to acquire the data byte from the addressed DPI module. The program may then execute OUT S' = 0 to specify a new DPI module, and if required, to transfer Z bits to that module, which again sets the Local Controller busy. When the Local Controller is not busy, the program acquires the data byte, and it may continue to issue OUT's, check the busy status, and acquire input bytes.

If the command word specifies a write operation, the first data byte to the DPI module is transferred by the OPR instruction. When the Local Controller goes not busy, the program may issue and OUT S' = 0 instruction to transfer a new data byte, and if required, new TA and DPI module addresses, and new Z bits. The program may continue to issue OUT instructions each time the Local Controller goes not busy.

Status information is accumulated by the Local Controller to reflect errors and alarms and to indicate the busy/not busy status of the Local Controller. It is transferred to the Arithmetic Unit by IN S' = 2. The busy status may also be checked by JNR S' = 0, and the presence of error indications may be checked with JNE S' = 0.

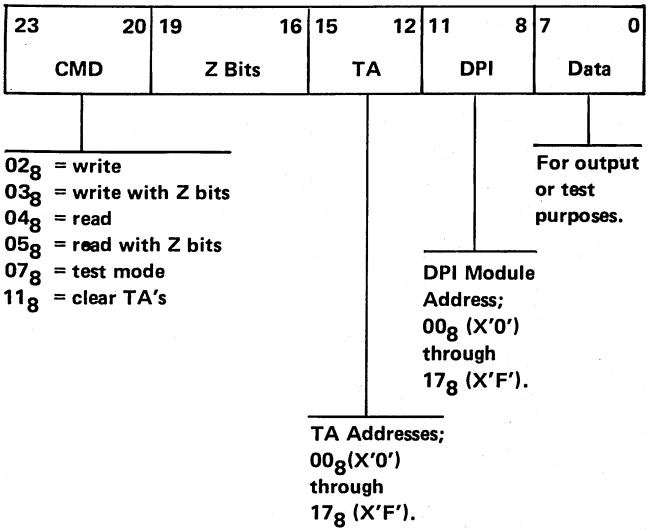
11.4.3 DPI Subsystem Instructions

In addition to the normal functions described under 4.5.2 in section 4 of the General Description, the following GEN 2 instructions, when addressed to the Local Controller, affect the DPI subsystem as described.

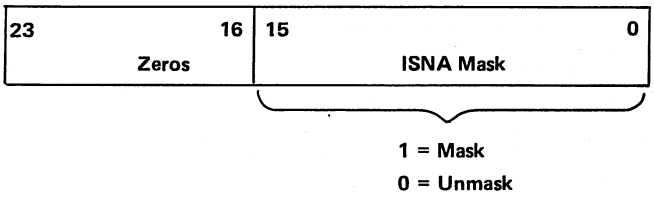
ACT S' = 6 = AIM - Activate interrupt mask. See 4.5.2.

ACT S' - 7 - DIM - Deactivate interrupt mask. See 4.5.2.

OPR S' = 0 = Initiate a transfer sequence. See 11.4.2. At the time of execution, the A Register contains the command word:

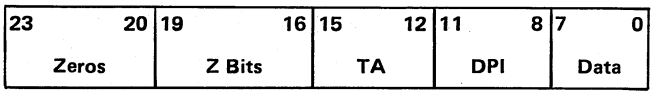


OPR S' = 1 - Transfer ISNA mask. This instruction is used to inhibit interrupts from TA's or consoles from which an Interrupt Status Not Available response has been received. See IN S' = 2. At the time of execution, the A Register contains the mask, each bit of which corresponds to a Termination Assembly or console:



ABT S' = 0 = Abort. Execution of ABT initializes the Local Controller and terminates any transmissions on the radials that may be in progress. Since an interrupted transmission could cause undefined results at the process interface, this instruction should be used only when no transmission in either direction is taking place. A Clear Termination Assemblies command (OPR S' = 0 with bit 23 of the command word set) can be used to clear out any information stored in the TA's without interrupting transmissions.

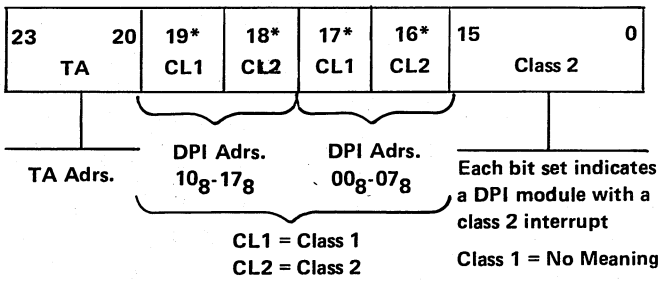
OUT S' = 0 = Transfer Z bits, TA address, DPI address and a data byte. This instruction can be executed anytime the Local Controller is not busy after OPR has transferred a command word. It can be used to transfer an output byte to a DPI module if the subsystem is in the write mode, or it can be used to change Z bits or addresses if the subsystem is in the read mode. At the time of execution, the A Register contains the following output word:



IN S' = 0 = Input a data byte. This instruction can be executed when the DPI subsystem is in the read mode and the Local Controller is not busy. It must be preceded by OPR or OUT if the Z bits or TA/DPI addresses are to be changed. The byte goes to bits 07 through 00 in the AU's A Register.

IN S' = 1 = Input Interrupt Data (INI). This instruction acknowledges an interrupt from a Termination Assembly or console and transfers the interrupt data word to the A Register. The content of the data word differs according to the type of TA:

Standard TA or console;

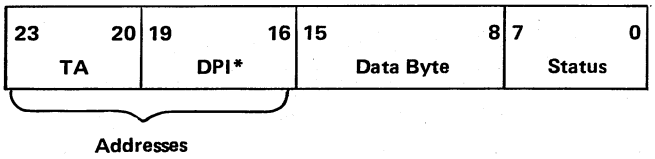


If bit 19 is set, one of the upper eight DPI modules in the TA has an interrupt.

If bit 17 is set, one of the lower eight DPI modules in the TA has an interrupt.

If bits 18 or 16 are set, one or more of bits 15 through 0 will be set to indicate which DPI module has a class 2 interrupt.

Sequence of Events TA;

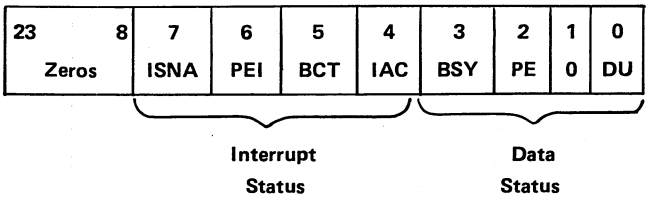


The data byte is data contained in the DPI module indicated by the address.

The status bits are zeros if the data was read successfully and are all set if the data was not read successfully for some reason such as a blown fuse or circuit breaker in a sensor power supply.

*These bits contain the TA address received by the controller if a type 1 API was requested.

IN S' = 2 = Interrogate Device Status (IDS). This instruction transfers the DPI subsystem status byte to the A Register and may be executed anytime. The status word has the following format:



The status bits have the following meanings:

ISNA; Interrupt Status Not Available. This bit is set if the Local Controller is unable to receive interrupt information from a scanned TA or console. Typically, the program would take the TA or console interrupt out of service by setting its bit in the ISNA mask via OPR S' = 1. The OPR instruction could be used to reset the mask bit after the malfunction is corrected.

PEI; a parity error was detected in the transmission of interrupt information from a TA to the Local Controller.

BCT; Wrong Bit Count. Interrupt information received from a TA did not have a correct number of bits in the data stream.

IAC; Interrupt Address Compare. The address returned from a TA in an interrupt information transmission was not the same as the TA or console that was polled.

BSY; Busy. The Local Controller is not ready to accept a new data or command word or is not ready to transfer data to the A Register in the AU. BSY also sets when IN S' = 1 is being executed to transfer interrupt information to the A Register.

PE; Parity Error. A parity error was detected by the Local Controller in a transmission from a TA or console.

DU; Device Unavailable. The addressed DPI module does not exist, or the TA or console's response for it was not received properly by the Local Controller.

Note: If the BSY bit is found reset while DU is set, the addressed DPI module did not respond properly, but the addressed TA did. Recovery may be attained by a new command. If both BSY and DU are set, the addressed TA or console did not respond within 50 microseconds, or did not complete its response. An incomplete response could be due to a parity error detected by the TA or console in the Local Controller's transmission, a failure or loss of power in the TA or console, or a nonexistent TA or console was addressed. Recovery from this situation may be attained by a new command or data transfer, or by a Clear Termination Assemblies command (see OPR S' = 0).

JNR S' = 0 = Jump if not ready. This instruction tests the Local Controller's busy status. If it is not busy (ready for data transfer), no jump takes place.

JNE S' = 0 = Jump if no error. Tests the Local Controller's error line which is true if any data status error bits are set.

11.4.4 Test Mode

If an OPR S' = 0 instruction is issued to the Local Controller with 07_8 in the CMD field of the command word, the Local Controller goes to the test mode, the busy bit sets, and the command, Z bits, addresses, and data are sent to the addressed TA or console, but not to the addressed DPI module. The TA or console immediately returns the data to the Local Controller, which then goes not busy. IN S' = 0 may then be executed to transfer the data byte to the AU for comparison. Other TA's or consoles may then be tested by issuing new OUT instructions and by executing IN S' = 0 when the Local Controller goes not busy.

11.5 ADDITIONAL FEATURES

Termination Cabinets. Standard 76" H x 30" D x 32" W cabinets. Require 115 Vac, ±10%, 47 Hz to 63 Hz, single phase, power; three wires (high, neutral, and safety ground). May include AL511 Power Surge Limiter.

Environmental Classes: Local Controller - A. Termination cabinets - A1. See 3.1.

11.6 SMALL DIGITAL I/O SUBSYSTEM

Small Digital I/O (SDIO) subsystems provide up to 128 process I/O points without necessitating an entire Digital Termination cabinet. Made of essentially standard Digital Process Interface subsystem elements, the SDIO package is usually housed in an ASU cabinet and consists of an AF501 Local Controller, a high density Termination Assembly, a 28 V power panel and associated cables.

11.6.1 Features

Termination Assembly Options. The SDIO Termination Assembly is available in two types:

AF301 Cable Connector Outputs

AF302 Terminal Strip Outputs

Process Module Options. Among the many module options which may be selected are: 28 V digital input or output boards, analog output generators, single point analog input boards, display drivers, and pulse train generators.

Software. Standard software for the Digital Process Interface subsystem Extended Digital I/O system is used with the SDIO.

Environmental Classes: Local Controller - A. Termination Assemblies - A1. See 3.1.

11.6.2 Capacity

Up to 64 of the 128 possible process I/O points may be outputs. Boards requiring isolated power and logic levels (TTL, etc.) may not be used. No power provisions have been made for 48 V or 125 V board options. A maximum of six analog generator output points may be used. Aside from these constraints, and provided that sufficient cabinet power is available, any of the standard modules listed in part 11.2 of this manual may be used.

ANALOG INPUT SUBSYSTEM

The APIA Series Analog Input Subsystem is one of several process interfaces in the TDC 4500 process control computer system. This subsystem is designed for flexibility and modularity, communication with process areas up to 2500 feet from the computer site over simple interconnecting cables, and an easy interface with a very large variety of process controls and sensors. Analog input data may also be received through the Data Hiway Interface module described in section 13.

The TDC 4500 process computer system acquires digital data which are representative of the magnitude and polarity of process variables, through the Analog Input Subsystem (AIS). Process variables, such as temperatures, pressures, fluid flow, Watts, Volts, Amperes, resistances, etc., are measured by sensors in the process, which provide analog voltage or current inputs to the AIS that are accurate representations of the process variables.

The AIS is capable of scanning up to 200 input points per second through two channels which consist of two serial data link cable-radials, each of which is up to 2500 feet in length. Each AIS can scan up to 2032 process inputs (2048 input points total). Where a scanning rate higher than 200 points per second is required, or where more than 2032 process inputs are needed, additional AIS's may be implemented.

12.1 FUNCTIONAL DESCRIPTION

As indicated on Fig. 12-1, the AIS consists of a Local Controller on the GENIE I/O Bus and one or more termination cabinets. The Local Controller serves primarily as a serial communications interface with the termination cabinets, which contain the majority of the subsystem's control logic. The running program furnishes instructions to the Local Controller that dictate each point to be scanned.

12.1.1 Local/Remote Controller Communication

The Local Controller has three program dictated modes of operation. In the normal mode, both channels are enabled and the Local Controller issues point scan requests to the remote controllers in the termination cabinets without regard to which channel the cabinet is on. The addressed remote controller accepts the message, selects the appropriate point, converts the analog data to a 12-bit plus sign digital data word, and returns the data to the Local Controller to be transferred to the Central Processor by the program. The second mode of operation is normally used only when a malfunction on a channel has made the channel inoperative. In the second mode, the Local Controller can communicate with the remote controllers on the operational channel, while the inoperative channel is removed from service for repair. The third mode is a test mode wherein Local Controller channel A is connected to Local Controller channel B, and the off-line test and diagnostic program can be used to test the Local Controller.

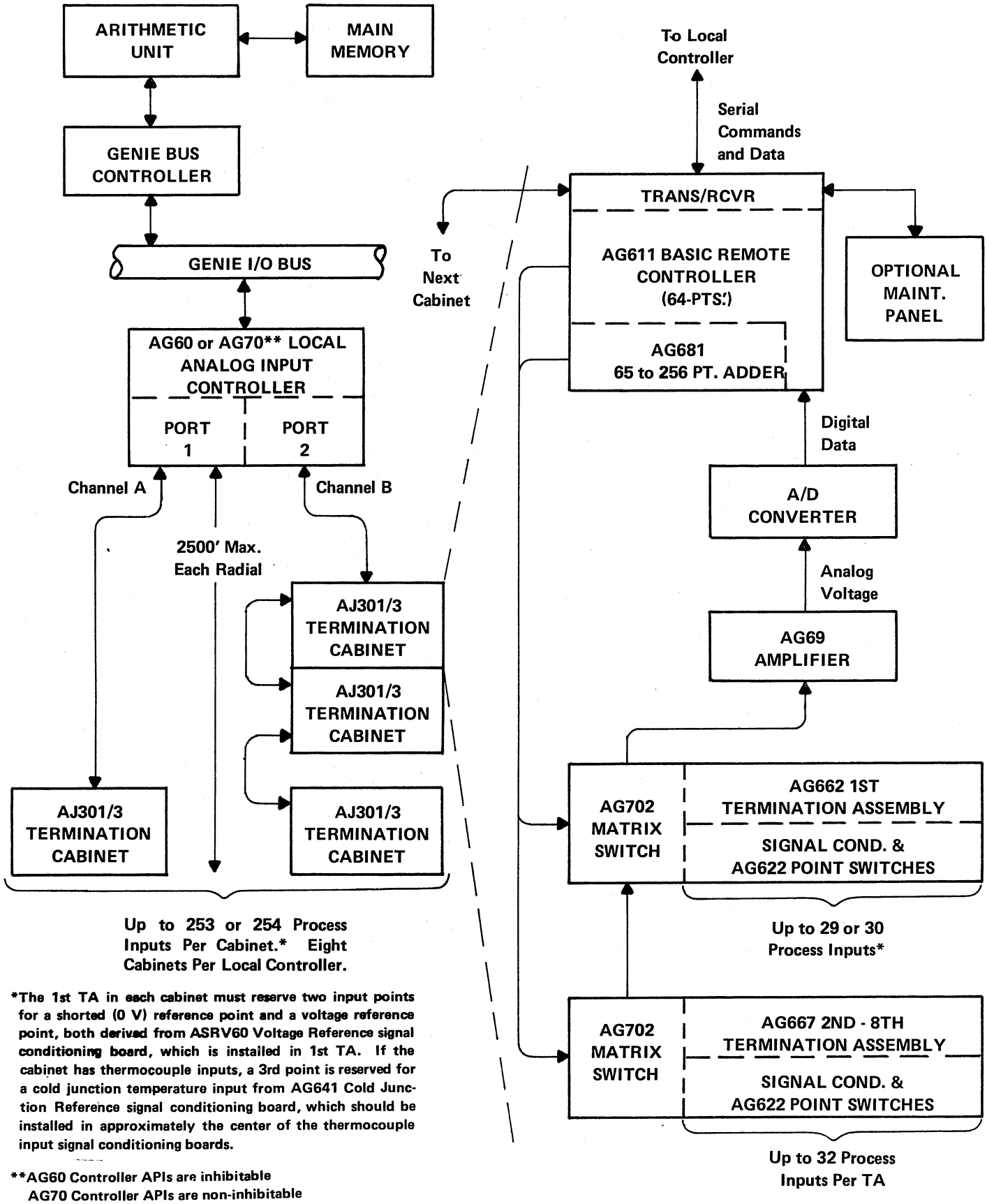
Except for the serial communications data, all remote controllers and the Local Controller are electrically isolated from each other, and each remote controller has its own power supplies and power monitor and sequencer, which remove the controller from the communications channel should the dc voltage be out of tolerance. Therefore, a malfunction in a remote controller will normally not affect other controllers, and if it does, its channel may be disregarded by the Local Controller until it is restored to service.

12.1.2 Analog Input Scanning

Each termination cabinet contains an input multiplexer consisting of the matrix switch and point switches on the Termination Assemblies (TA's) in the cabinet. The point switches select the analog inputs using a form C "flying capacitor" switching scheme, wherein the capacitor is connected to the conditioned analog input voltage when the point switch is at rest, and when it is selected, the capacitor is disconnected from the input and reconnected to the analog input amplifier, via the matrix switch. The capacitor retains its charge while it is switched, and the very high input impedance of the amplifier does not discharge it, so the input to the amplifier is representative of the magnitude of the process variable, but any common mode voltage present at the input point is not applied to the amplifier.

The AIS accepts the following as standard inputs:

- Voltages with full scale values as low as $\pm$10 millivolts and as high as $\pm$500 Volts.
- Currents ranging from 0.25 mA to 50 mA.
- Bridge Circuit Resistances in the range from 9.5 ohms to 1050 ohms.
- Thermocouples of any type. Thermocouple wires may be directly connected to the Termination Assemblies for conditioning by thermocouple input signal conditioning boards. AG641 Cold Junction Reference signal conditioning board is required to provide a standard reference temperature input to allow



*The 1st TA in each cabinet must reserve two input points for a shorted (0 V) reference point and a voltage reference point, both derived from ASRV60 Voltage Reference signal conditioning board, which is installed in 1st TA. If the cabinet has thermocouple inputs, a 3rd point is reserved for a cold junction temperature input from AG641 Cold Junction Reference signal conditioning board, which should be installed in approximately the center of the thermocouple input signal conditioning boards.

**AG60 Controller APIs are inhibitable
AG70 Controller APIs are non-inhibitable

Fig. 12-1 Analog Input Subsystem

the program to correct for the conversion from thermocouple wire to copper wiring at the input point. A High Precision unit (model AG651) is available to make the conversion externally to the cabinet (see 12.2.5).

Each point switch board accommodates up to four points and is associated with a signal conditioning board with four identical signal conditioning circuits (see 12.2.4). The signal conditioning circuits filter and may attenuate the input signal to produce an analog voltage input to the amplifier that is within the full scale range of the amplifier (see 12.2.3). Maximum accuracy is attained when the input is as near to the full scale value as practicable.

12.1.3 Analog Input Parameters

The terms used in the accuracy statements are defined in Appendix A to this General Description and on drawing no. 70A121205. When properly maintained and when the standard offset error correction methods are used by the software, the accuracy and principal parameters of the AIS are:

- Scanning Speed: 200 randomly scanned points per second.
- Point Switching: Form C.
- Digital Data Word Resolution: 12 bits plus sign.
- Subsystem Gain Error: $\pm$0.025% of full range, +5 μv, RTI.
- Repeatability Error: $\pm$.025% of full range, $\pm$10 μv, RTI.
- Crosstalk Rejection: 120 db minimum from dc to 60 Hz.
- Gain Error Temperature Coefficient: $\pm$0.0045% of full range per $^{\circ}$C.
- Common Mode Voltage Rejection Ratio: 10^6:1 minimum, at a gain setting of 1000:1. Maximum common mode voltage at any input termination point is $\pm$250 Vdc or 500 V peak to peak at 60 Hz.

12.2 AIS OPTIONS

12.2.1 Analog Input Termination Cabinets

The AG60 or AG70* Local Analog Input Controller on the GENIE Bus can accommodate up to eight analog input termination cabinets, each of which serves as a remote station along one of the communication channel radials. Each termination cabinet can accommodate up to 254 process input points, plus a shorted reference point and a voltage reference point, through up to eight Termination Assemblies. The AG611 Basic Remote Controller in each termination cabinet selects up to 64 input points. An AG681 65 to 256 point adder may be implemented in the basic controller to serve up to 192 additional input points.

If no thermocouple inputs are connected to the input terminations in a cabinet, the AJ303 Combination Digital and Analog Termination Cabinet may be shared by the AIS and the DPI subsystem (section 11). The number of Termination Assemblies for either subsystem which may be implemented in the AJ303 cabinet is determined by the mix of low, medium, and high density Digital I/O Termination Assemblies present. Cabinet space required by the TA's for either subsystem is defined in the TDC 4500 Configuration Guide.

The AJ301 Termination Cabinet is for analog inputs only, and can accommodate up to eight 32-point Termination Assemblies.

12.2.2 Termination Assemblies

The first Termination Assembly implemented in a termination cabinet is model AG662 if the process inputs are to be made to screw type terminals or model AG665 for process connections via cable connectors. Subsequent TA's, to a total of eight TA's per cabinet, are model AG667 for screw type terminals or model AG668 for cable connectors. Each TA must implement one AG702 Matrix Switch and may implement up to eight 4-point switches. Each point switch board is paired with a signal conditioning board (12.2.4).

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*APIA1 (AG60) APIs are inhibitable
APIA2 (AG70) APIs are non-inhibitable

12.2.3 Analog Input Amplifier

The analog input amplifier amplifies the output of the signal conditioning circuit to an appropriate input for the A/D converter. The full scale input voltage to the A/D converter is 10.00 Volts, and maximum accuracy is attained when the input is as near the full scale input as possible. Both fixed gain amplifiers and programmable gain amplifiers are available. The gain of the programmable amplifier is specified by the program in each point scan request.

- AG691 Programmable Gain Amplifier:

Gain	Full Scale Input
1000:1	10 mV
500:1	20 mV
250:1	40 mV
125:1	80 mV
62.5:1	160 mV

- Fixed Gain Amplifiers:

Model	Gain	Full Scale Input
AG692	1000:1	10 mV
AG693	500:1	20 mV
AG694	250:1	40 mV
AG695	125:1	80 mV
AG696	62.5:1	160 mV

12.2.4 Signal Conditioning

Up to eight point switch boards are installed in each TA and each point switch is paired with a signal conditioning board containing four identical signal conditioning circuits. The signal conditioning circuits convert the input sensor signal to a millivolt range voltage suitable for input to the analog input amplifier. Standard signal conditioning boards of the following types are available. Refer to drawing no. 70A122720 for detailed specifications for the signal conditioning boards and to the TDC 4500 Configuration Guide for model numbers and configuration information.

3010ASFL Filter, ±10 mV to ±640 mV

3010ASAF Attenuator, to ±500 V

3010ASIM Current Input, to 50 mA

3010ASOT Thermocouple Input with Open TC Detector

3010ASRT Resistance Bridge (RTD) Inputs

3010ASAP63 Slidewire Inputs (includes power distribution and fuse. 125:1 attenuation ratio).

12.2.5 Thermocouple Inputs

Where thermocouple wire is connected to an input Termination Assembly, the connection itself forms a thermocouple, which affects the input to the AIS but can be compensated for by the software, if the termperature of the termination is known. Where thermocouple inputs are connected to a TA, one of the signal conditioning boards in the cabinet must be an AG641 Cold Junction Reference board. This board should be located in the approximate center of all thermocouple signal conditioning boards so that the temperature will be reasonably representative. The first input from the AG641 board is the reference temperature analog input signal. The accuracy of the reference temperature input is ±2°C.

A more precise reference temperature may be attained through the use of an AG651 Thermocouple Termination Reference assembly. This unit is designed for wall mounting outside the termination cabinets and accepts up to 63 thermocouple inputs. The 63 input signals and the reference temperature signal are connected to one or two TA's in a termination cabinet via copper wire cables up to 999 ft. in length. The accuracy of the reference temperature input is ±0.5°C.

All thermocouple input signal conditioning boards include an open thermocouple detection feature wherein the data word returned to the Central Processor after an open thermocouple is scanned, indicates the open condition to the program. Signal conditioning board model 3010ASOT6 uses a long life battery in its detector, while model 3010ASOT70 detects open thermocouples electronically. When electronic open thermocouple detection is used, an AG631 Electronic Open Thermocouple Control board must be added to the AG611 Basic Remote Controller module in the termination cabinet.

12.3 OPERATING SEQUENCE

To initiate the selection and conversion of an analog input point, the program executes an OUT instruction addressed to the AIS Local Controller, which transfers a command word to the Local Controller. The Local Controller then goes busy, transmits the command to the appropriate remote controller, and awaits its reply. When the converted data is received in the Local Controller, it goes not busy, and generates an operation complete API. The program may then issue an IN instruction to the Local Controller, which transfers the input data and status word to the A Register.

The Local Controller uses one GENIE Bus device address and generates two API's. The type 0 API is generated when the Local Controller has a data/status word ready for transfer to the AU, with no error bits set. The type 1 API is generated when the controller completes the operation but an error has been detected, or when it is unable to complete an operation and its 10 millisecond deadman timer has timed out.

12.3.1 AIS Instructions

In addition to the normal function described under 4.5.2 in section 4 of this General Description, the following GEN 2 instructions, when addressed to the Local Controller, affect the AIS as described.

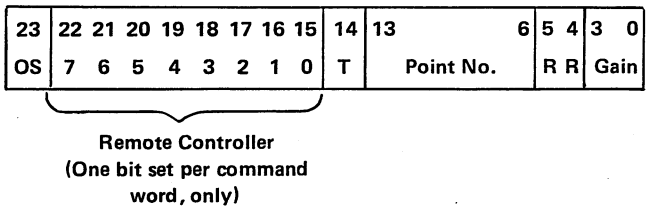
ACT S' = 0 = Activate API. If the Local Controller's error line is false, the type 0 API is generated, if the error line is true, the type 1 API is generated. This instruction is ignored if the Local Controller is busy.

ACT S' = 6 = AIM - Activate Interrupt Mask. See 4.5.2.

ACT S' = 7 = DIM - Deactivate Interrupt Mask. See 4.5.2.

ABT S' = 0 = Abort. ABT sets the Local Controller busy for 10 milliseconds, after which it goes not busy, and initializes. The 10 ms delay allows any operation in progress to run to completion.

OUT S' = 0. OUT transfers a command word to the Local Controller and initiates an AIS operation. It clears any alarm or API indications. The command word in the A Register at the time of execution has the following format:



OS = Open Thermocouple Detector Sensitivity Bit (non-battery detectors, only). If this bit is set, high sensitivity is requested. If reset, low sensitivity.

T = Test Bit. This bit when set, forces a "Wrong Remote Respond" alarm and an open thermocouple alarm, for test and diagnostic purposes. Normal data is available when the operation is complete.

Point No. = 000_8 to 377_0, or any point number from 0 256_{10} on the remote controller.

RR; these bits are reserved for possible future use.

Gain; specifies the gain, if the remote controller has a programmable gain amplifier.

00_8 = 62.5:1.

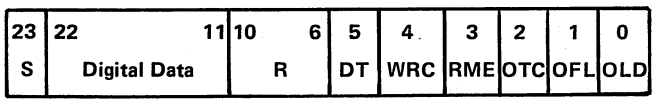
01_8 = 125:1.

02_8 = 250:1.

03_8 = 500:1.

04_8 = 1000:1.

IN S' = 0 = Input Data/Status Word. IN is executed when the Local Controller goes not busy or in response to an operation complete API. It transfers the following data and status word to the A Register in the AU:



S = Data Sign Bit. If the sensor input is positive, the data is in straight binary form. If the input is negative, the data is in 2's complement form.

R = Reserved for possible future use.

DT = 1 = Deadman Time-Out. Either the selected remote controller detected an error in a transmission from the Local Controller, the remote controller does not exist, or it has had a malfunction or power failure. The transmission from the Local Controller includes a check segment based upon the polynomial $1 + X^2 + X^5$, which is checked by the remote controller.

WRC = 1 = Wrong Remote Controller. The remote controller that responded was not the one selected.

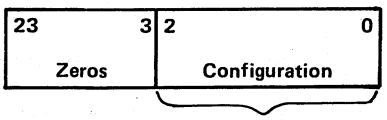
RME = 1 = Received Message Error. The Local Controller detected an error in the transmission from the selected remote controller. Either it was a check segment error or the content of the message was wrong. The remote controllers transmit a $1 + X^2 + X^5$ check segment for checking by the Local Controller.

OTC = 1 = Open Thermocouple. An open thermocouple was detected on the selected point. This bit sets when the detector is the non-battery type only. If bit 23 of the command transferred by OUT was equal to 1, OTC sets if the thermocouple resistance is greater than 300 ohms. If bit 23 of the command equals 0, OTC sets when the resistance of the thermocouple is greater than 1000 ohms. Open thermocouples detected by battery-powered detectors cause an overflow (OFL).

OFL = Overflow. The input to the A/D converter exceeded the full range and over-range limits of the converter, i.e., the input exceeded +10.2400 V or -10.2375 V. Polarity at the input of the converter is inverted from that of the sensor input. Overflow occurs if a battery-powered open thermocouple detector detects an open thermocouple.

OLD = Overload. More than one point relay was selected in the Termination Assembly.

OPR S' = 0. This instruction is used to set up the Local Controller to isolate the two radial channels or to transmit to each other. It also may be used to return the channels to normal operation. When the system hardware is initialized or when an ABT instruction is issued to the Local Controller, the normal configuration is set up. The content of the A Register when OPR is executed defines the port configuration:



0_8 = Channels A and B transmit and receive normally.

1_8 = Channel A, only, transmits and receives.

2_8 = Channel B, only, transmits and receives.

3_8 = Channel A transmits and Channel B receives for test and diagnostic purposes.

4_8 = Channel B transmits and Channel A receives for test and diagnostic purposes.

The two isolation configurations (1_8 and 2_8) are used when a channel malfunction causes erroneous data to be received by the Local Controller, which it must ignore. The test configurations (3_8 and 4_8) are used to connect the two channels to allow testing of the Local Controller without the need of a remote controller. The hardware compares the transmitted and received data and sets the Local Controller error line true if they do not compare.

JDR = Jump if Data Ready. See 4.5.2.

JCB = Jump if Channel Busy. See 4.5.2

JNE = Jump if No Error. This instruction tests the Local Controller error line, which is true if any of the error conditions in the input data/status word are true (see IN S' = 0) or if an error is detected in the test configuration (see OPR S' = 0).

12.4 ADDITIONAL FEATURES

Termination Cabinets. Standard 76" H x 30" D x 32" W cabinets. Require 115 Vac $\pm$10%, 47 Hz to 63 Hz, single phase, power; three wires (high, neutral, and safety ground). May include AL511 Power Surge Limiter.

Environmental Classes: Local Controller - A - Termination cabinets - A1. (See 3.1).

Modern process computers often need to communicate with other process computers and with information systems. Data links often exist between process computers where two or more such systems are involved in the control and monitoring of a process and one can take at least some functions of another system in case of a failure. In some cases, two process computers may operate as redundant systems, where one is on line and controlling the process and the other is updated periodically over a data link, so that it can take over, if the on-line system fails. Still another application for data links is in the transmittal of data from a process computer involved in control and monitoring of a process to another process computer or an information system performing supervisory functions over several process control systems.

13.1 ASYNCHRONOUS COMMUNICATION DRIVE

The AXPV1 Asynchronous Communication Drive (ACD) provides communications through data sets over telephone lines or other communications media. It may also be directly connected to another ACD or equivalent interface in another process computer by up to 50 feet of cable. It provides bit-serial, asynchronous-character communications via an EIA RS232C interface with the local data set (or the opposite terminal if directly connected), at a baud rate from 110 to 1800 bits per second. The AH401 Data Set (300 baud), the AH401-3 Data Set Adder (300 baud - a second data set in the rack provided by AH401), the AH402 Data Set (1200/1800 baud), and the AH402-3 Adder (1200/1800 baud - a second data set in the rack provided by AH402) are intended for use with the ACD. These data sets may be installed in an auxiliary system cabinet or they may be freestanding. Maximum ACD to data set cable length is 50 feet.

13.1.1 Data Format

Communication through the ACD may be simplex, half-duplex, or non-simultaneous full-duplex, as determined by the data sets, the communications medium, and the computer program.

While data may be transferred through the ACD by means of the GEN 2 instruction, OUT, and IN, the TIM/TOM feature is the principal means of data transfer. Data are transferred to, and from, a table area in main memory when using TIM/TOM, or the A Register, when using GEN 2 instructions. The ACD transmitter (output channel) converts each eight bit parallel output character to a ten or eleven bit serial character for transmission by the data set. The ACD receiver (input channel) converts each ten or eleven bit serial character received by the communications device to an eight bit parallel character. Each bit of a serial character occupies one unit of time. The reciprocal of the duration of the bit time is the baud rate of the communications channel. The serial characters consist of a start bit, seven data bits, a parity bit, and at least one stop bit. In the quiescent state, both the input and output serial data lines are in the marking state. The advent of a character is indicated by a bit time when the line goes to the space state. The eight data and parity bits follow the start bit. The stop bit time is the minimum time that the line must remain in the marking state before a new character may be transferred. Several data formats are available as described in the following:

1. The transmitted character format is set up under program control when the output channel is activated see 13.1.7). The character format may be 8-bit binary, or 7-bit plus parity ASCII or EIA (EIA is not implemented in standard software). Transmitted parity bits are generated by the ACD. The ACD appends the parity bits, as dictated by program instructions transferred to the ACD by means of the GEN 2 instruction, OPR. When in the binary mode, no parity bit is appended. When in the ASCII mode, even parity is appended in character channel 8. When in the EIA mode, odd parity is appended in character channel 5. Either one or two stop bits are appended to each transmitted character, as selected by a jumper pin on the transmitter.

2. The expected received character format is dictated by program instructions transferred to the ACD by means of OPR (see 13.1.7). When in the binary mode, eight binary data bits are transferred to the AU and memory. When in ASCII or EIA modes, the parity bits and data are transferred from the appropriate character channels, with appropriate polarity, to the parity checking logic in the ACD. (EIA is not implemented in standard software). A jumper pin is provided on the ACD receiver to select the transfer of ASCII or EIA character parity bits to the AU and memory, if required.

13.1.2 Timing

The ACD operates at 110, 150, 300, 600, 1200, 1800, 2400, 4800, 7200, or 9600 baud, as selected by jumper pins on the module.

13.1.3 Received Character Recognition

The ACD receiver recognizes the following characters in the input data stream, as end-of-message characters when activated in the indicated format. Upon receipt of such a character, the receiver terminates the current operation, goes "not busy" and an end-of-record API is generated as the character is transferred to the Central Processor. The ACD transmitter does not employ character recognition.)

1. ASCII; EOT(004_8), ENQ(005_8), ACK(006_8)*, NAK (025_8)*, the character following ETX(003_8), the character following ETB(027_8), and any ASCII numeral (060_8 to 077_8) following DLE(020_8).

2. ASCII teletypewriter characters; NUL(000_8), CR (015_8), CAN(030_8), EM(031_8), SUB(032_8), and ESC (033_8)**, release of the BREAK key (causes an alarm), plus the ASCII characters indicated above.

3. EIA; CR(100_8). Odd parity is assumed in channel 5 of the received character.

13.1.4 Current Loop

The ACD drive also contains a full-duplex 20 milliamp neutral current loop suitable for use with Teletype Corporation's model 33 or 35 teleprinters and similar equipment. The current loop cable is made of two twisted wire pairs and may be up to 1000 feet long.

13.1.5 Automatic Answering

When a ring signal is received on the data set interface while the ACD transmitter is not busy, the transmitter generates and end-of-record interrupt, which indicates to the program that a call is incoming. The program responds by issuing an appropriate instruction to activate the ACD (see 13.1.7). The ACD transmitter goes busy during the ring signal (approximately 600 milliseconds).

13.1.6 Line Turnaround

The ACD automatically changes from transmission to reception or from reception to transmission, under program control. When used with half-duplex data sets with line turnaround capability, the requirement for a change in direction is detected by the receiver by sensing the received carrier on/off status, and the change is implemented by OPR instructions issued by the program (13.1.7).

*ACK and NAK are recognized as end-of-message characters only when outside the text or header of an incoming message.

**The end-of-message status may also be generated on the first character following an ESC (by jumper option).

13.1.7 ACD Instructions

The following GEN 2 instructions affect the ACD transmitter: ABT, JCB, JDR, JNE, OPR, and OUT. ABT, IN, JCB, JDR, JNE, and OPR affect the receiver. (Refer to 4.5.2 and Appendix C.) OPR instructions issued to the transmitter and the receiver have special functions as described in the following:

1. OPR addressed to the ACD transmitter transfers control words to the transmitter which activate and deactivate the transmission of data, dictate the ACD line control state, and dictate the transmitted character format. The following octal codes in the A Register when OPR is executed set up the condition indicated;

   050_8 - Answer and/or hold line for receiving.

   060_8 - Answer and/or hold line for transmitting.

   064_8 - Answer and/or hold line for transmitting and activate data transfer in ASCII.

   065_8 - Answer and/or hold line for transmitting and activate data transfer in ASCII (teletypewriter).

   066_8 - Answer and/or hold line for transmitting and activate data transfer in binary (no character recognition).

   067_8 - Answer and/or hold line for transmitting and activate data transfer in EIA.

   004_8 - Activate data transfer in ASCII.

   005_8 - Activate data transfer in ASCII (teletypewriter).

   006_8 - Activate data transfer in binary (no character recognition).

   007_8 - Activate data transfer in EIA.

   040_8 - Abandon call (hang up).

   100_8 - Deactivate data transfer.

   140_8 - Deactivate data transfer and abandon call.

   150_8 - Deactivate data transfer, answer and/or hold line for receiving.

   160_8 - Deactivate data transfer, answer and/or hold line for transmitting.

2. OPR addressed to the ACD receiver transfers control words to the receiver which activate and deactivate the reception of data, instruct the receiver to generate an end-of-record interrupt when the received carrier is on or comes on, or instruct the receiver to generate an end-of-record interrupt when the received carrier is off or when it goes off. The control words also dictate the received character format:

   000_8 - Sense carrier on.

   004_8 - Activate data reception in ASCII.

   005_8 - Activate data reception in ASCII (teletypewriter).

   006_8 - Activate data reception in binary.

   007_8 - Activate data reception in EIA.

   100_8 - Sense carrier off, deactivate data reception.

13.1.8 Additional Features

Device Addresses and API's: The ACD uses two GENIE Bus device addresses (transmitter and receiver) and generates four API's (2 data exchange and 2 end-of-record). Receiver API's have the higher priority and the receiver EOR API may be generated either when recognized or when read into the CPU.

Environmental Class: A (See 3.1.)

13.2 DATA HIWAY INTERFACE (DHI)

The TDC 4500 Data Hiway Interface (DHI) is a GENIE Bus plug-in option which gives the computer preferred access to a TDC Data Hiway (see Fig. 13-1). Primarily, it allows the host computer to communicate directly with TDC 2000 and TDC 7100 Data Hiway devices for process data acquisition and control purposes.

The interface accepts 24-bit computer words from the CPU memory or A Register and appends the seven bits required for the Data Hiway words, including the BCH code bits. It produces a 31-bit serial-asynchronous Hiway transmission at a bit rate of 250 kHz. Conversely, the interface will accept Hiway words, at the same rate, and assemble 24-bit words, for Direct Memory Access (DMA) transfers to CPU memory. Interrupts are generated on conclusion of message transfer or error detection.

The Data Hiway may be connected to 63 other Hiway devices (including 28 "polled" devices), when the system includes a Hiway Traffic Director (HTD), or up to a total of 24 devices without the HTD. In the latter case, this interface will partially assume the role of the traffic director. The interface includes dual Hiway ports which are program selectable. The maximum distance (cable length) between the DHI and the HTD is one mile.

All of the DHI hardware (logic) and firmware (microprogram) is contained on two printed wire boards (PWBs) which occupy three adjacent card slots in the GENIE Bus chassis. And inter-PWB signal cable connects the "D" fields (front edge) of both boards. A connector adaptor, attached to the GENIE backpanel, provides connections for the Hiway cables and HTD signal lines.

All DHI options are exercised using pin jacks and plugs or dual-in-line-package (dip) sockets and switches, all of which are located on the component side of the PWAs.

The DHI (model number AIDH11), hereafter also called the interface, is similar to and serves the same purpose as the 4DP4400AE44 Hiway Interface Module (HIM) which is a member of the HS4400 product line.

13.2.1 Data Formats

Figs. 13-2 through 13-5 illustrate the relationships between the Data Hiway word formats and the TDC 4500, CPU word formats for the transmission and reception of Command words and Data words. The destination address and data field formats are dependent on the Hiway device (PIU, controller, operator station, etc.) with which the interface is communicating. Here is a brief description of the Hiway commands and message transaction protocol:

- COMMAND READ is used by one Hiway device to request a specific word of data from another Hiway device.

- COMMAND WRITE is used by one Hiway device to precede the data which it intends to send to another Hiway device. The data can be a single word or a block of words.

- CALL-UP is used to "loan" the Hiway to a non-preferred access Hiway device which responded to a POLL. A response is expected.

- POLL is issued periodically to allow recognition of Hiway devices desiring access to the Hiway to report significant changes, alarms, etc. Where the HTD is

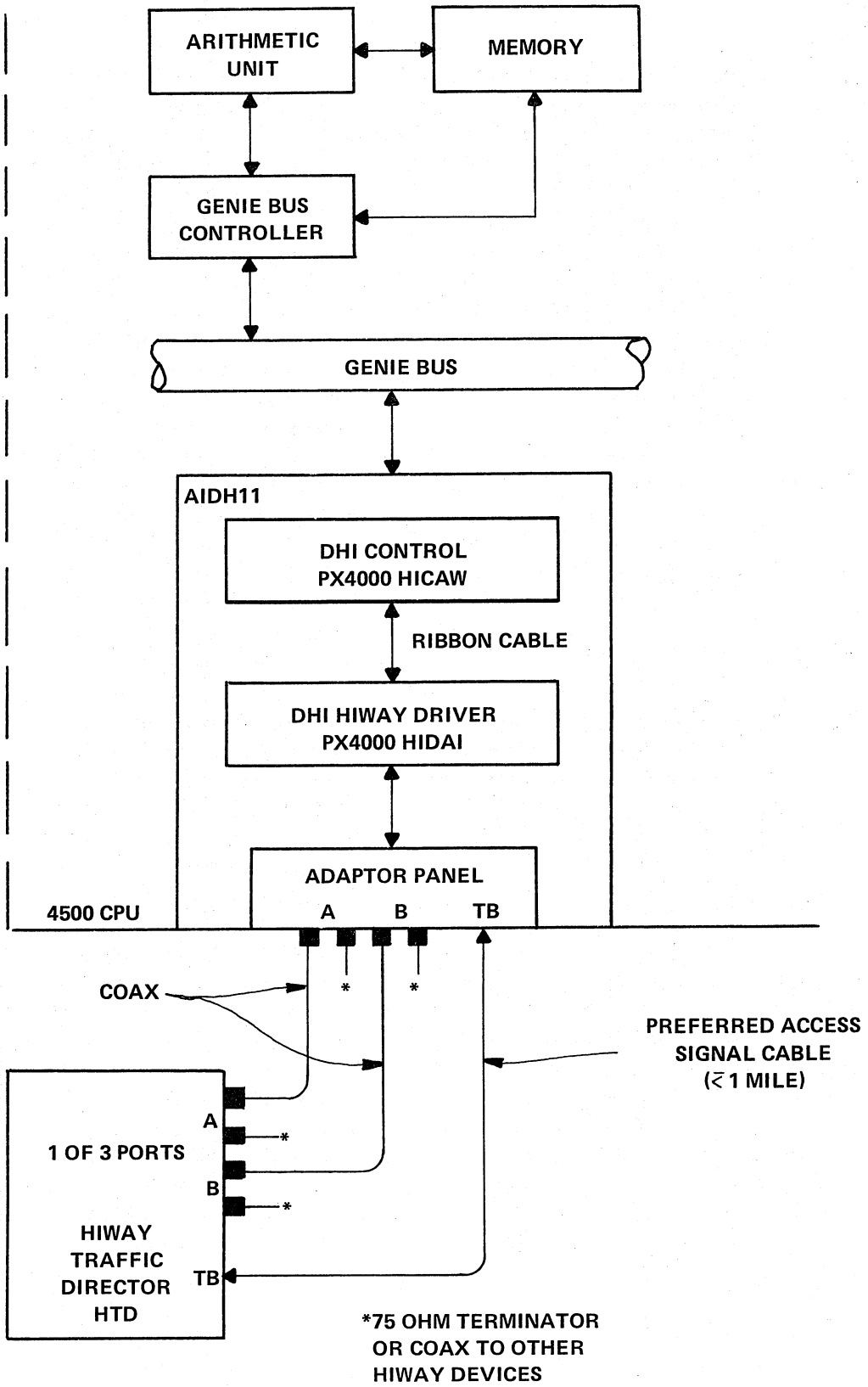


Fig. 13-1 DHI System Interface

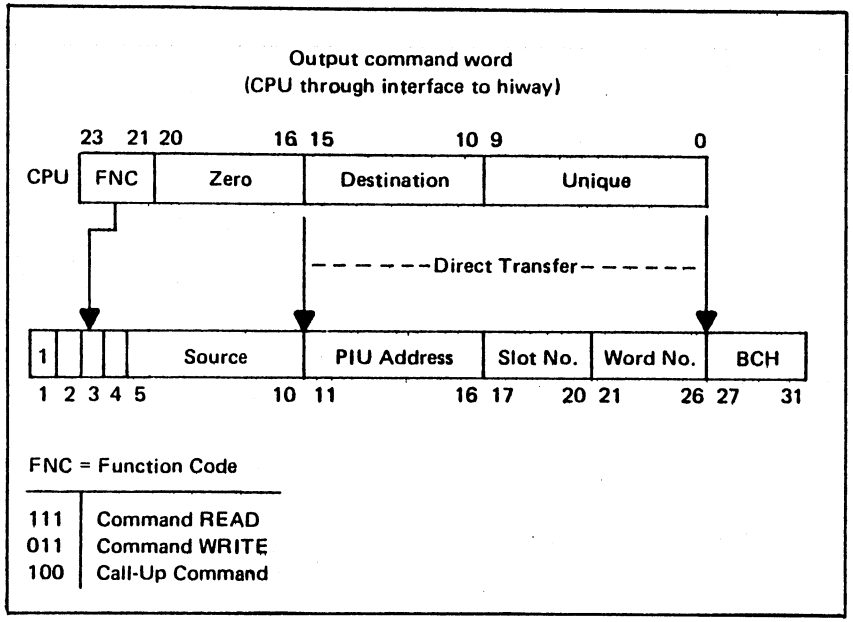


Fig. 13-2

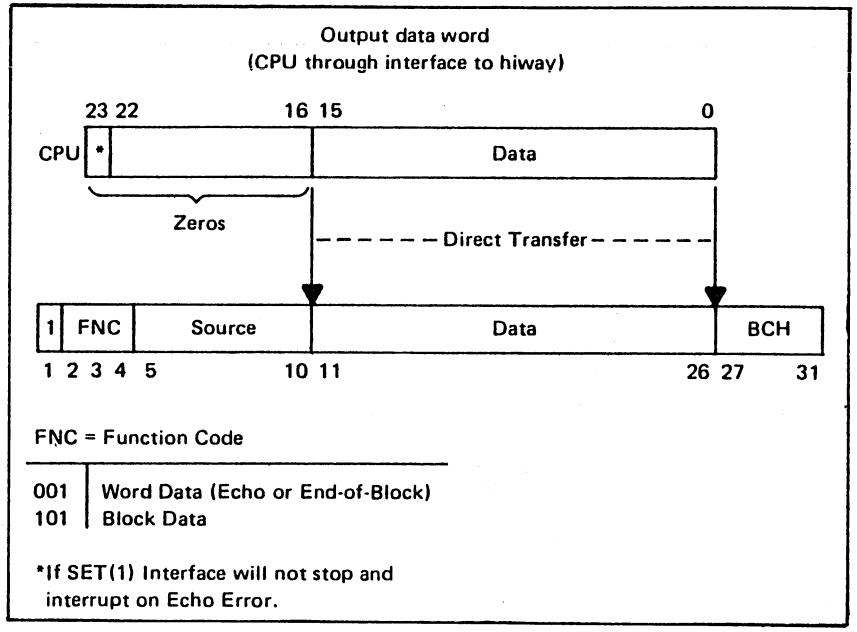


Fig. 13-3

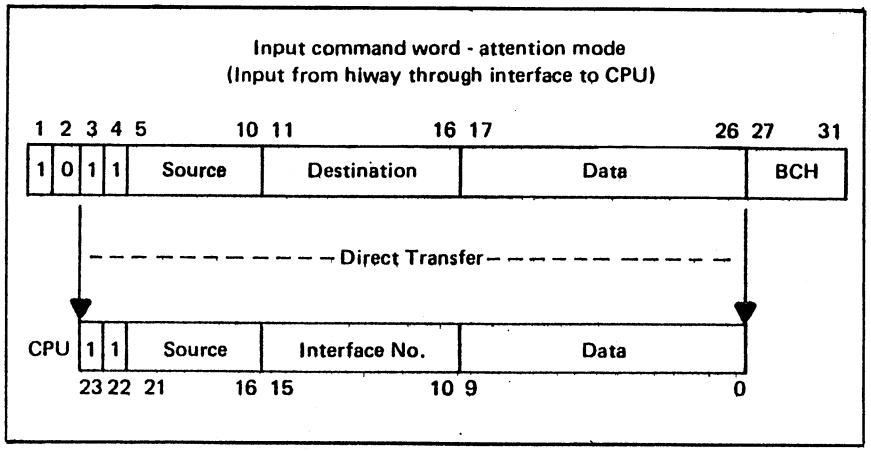


Fig. 13-4

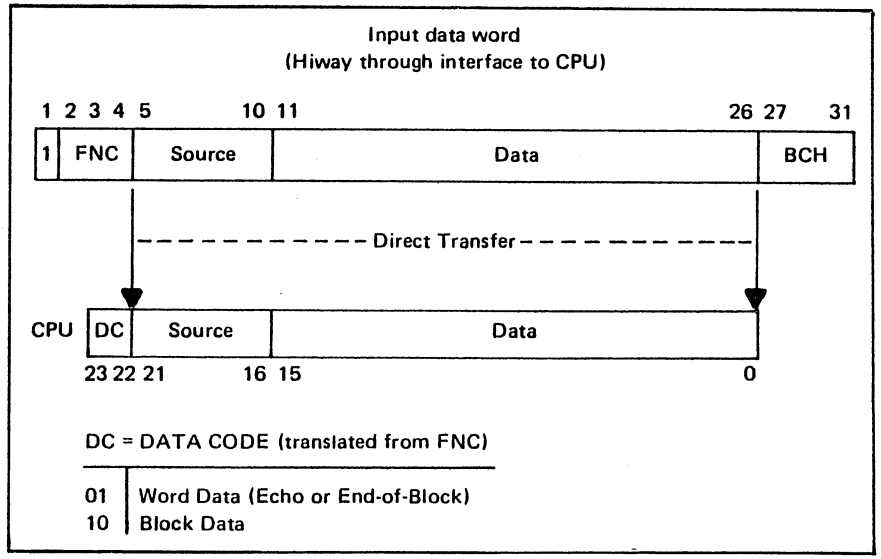


Fig. 13-5

not part of the Hiway system, the interface automatically performs the POLL function about every 15 milliseconds, unless it is in the "listen only" mode.

- BLOCK DATA is used to signify the sequential transfer of multiple data words. All except the last data word in the block will carry the 101_2 function code. The interface range is limited to 70 words.

- WORD DATA is used to signify the transfer of single data words, or for the last word in a block of data (see Block Data). When a Hiway device receives a data word in this format, it returns the word to the source device as an ECHO verification.

- BUSY is generally used as a response to a command word when the requested action cannot be taken or the requested data cannot be provided. If data cannot be accepted by a receiving device, it returns BUSY in lieu of the ECHO. The exact meaning of a BUSY response depends on the sending device and must be interpreted by the user. The interface always interrupts the CPU with an error flag set when this response occurs in the preferred access mode.

13.2.2 Modes of Operation

Two basic modes of operation are provided: Preferred Access and Attention (accept unsolicitated data). Either mode is selected and initiated by computer software using micro-coded GEN 2 instructions (see CPU Instructions).

13.2.2.1 Preferred Access Mode

Operation in this mode is "table driven", that is, all COMMAND data and WORD data are stored in and read from CPU memory tables, referred to as Command tables and Data tables. The data table is used for both supplying WRITE data words and for storing READ data words. Memory table starting address and range parameters must be given to the interface prior to each Hiway transaction.

After gaining preferred access to the Hiway, the interface will transmit the first Command word, which informs the addressed Hiway device that data is to follow (COMMAND WRITE), that data is requested (COMMAND READ), or that it must perform a specific task (CALL UP). The interface will then process (send or accept) the related data or provide appropriate error status indicating why not.

When the memory table range has been exhausted, or a sequence or response error has been detected, the interface relinquishes the Hiway and generates a CPU interrupt. The CPU program must interrogate the error/status word to determine the cause of the interrupt.

The types of operation performed in the preferred access mode are:

List (Single Word Transfers) - For a contiguous sequence of "single-response" command/transactions over the Hiway. The CPU memory command table and data table must have a one-for-one relationship. The command table may contain a mixture of READ and WRITE commands; likewise, the data table may contain data words (WRITE) and spaces for READ WORDS, including ECHO.

Operation is started with OUT S' = 1 which transfers the starting memory address of the command table from the A Register to the interface buffer. Prior conditioning of the memory data table starting address (OUT S' = 2) and range (OUT S' = 3) words in the interface buffer is required.

Operation terminates on memory table range exhaustion, or error. In either case, the interface will relinquish Hiway access, update its error status word and generate a type 0 interrupt.

Block (block Transfers) - For single block transactions over the Hiway. Operation is started with an OPR S' = 7 which transfers a single command word from the A Register to the interface. A memory command table is not required. Prior conditioning of the memory data table starting address (OUT S' = 2) and range (OUT S' =3) words in the interface buffer is required.

If the command was WRITE, data words are extracted from the data table for transfer. The last word is sent in the word data (end-of-block) format. The interface waits for ECHO from the receiving device before terminating.

If the command was READ, the interface stores each word in memory as they are received from the sending device. The operation terminates upon detection of end-of-block data word (or range exhaustion), or error.

Call-Up - Operation is started with an OPR S' = 7 which transfers a single command word from the A Register to the interface. Prior conditioning of the memory data table starting address (OUT S' = 2) and range (OUT S' = 3) words in the interface buffer is required.

If the response is COMMAND WRITE followed by data (block) words, the interface stores each word in the memory data table as received from the sending device. When the end-of-block is detected, an ECHO is returned to the sending device, provided the range has not been exceeded.

Polling - If the interface is optionally performing the POLL function, it transmits the POLL word about every 15 milliseconds. Any Hiway device may respond by sending a single pulse back to the interface following the POLL word. The interface assembles all responses, which appear in dedicated time slots, into a 24-bit poll-response word. The CPU program can transfer this word to the A Register for interrogation with the IN S' = 6 instruction. The interface generates a type 1 non-inhibitable interrupt only if there has been a response to the POLL word.

13.2.2.2 Attention Mode

In the attention mode, the interface may receive unsolicitated data from any Hiway device which is capable of initiating COMMAND WRITE transactions. The interface will DMA transfer the command and its associated block of data into the CPU memory table. On end-of-block or range exhaustion, the interface will generate a type 1, non-inhibitable interrupt, and, it also updates the error/status word.

The attention mode feature is especially useful when the system includes TDC 7100 PIUs which process I/O signals continuously and report only when unusual changes of significant events occur, thus, relieving the host computer from the burden of monitoring reasonably well-behaved points.

There are actually two attention modes of operation: Normal attention and Listen Only. If the system does not include a Hiway Traffic Director (HTD), the normal attention mode cannot be used.

Normal Attention Mode

The normal attention mode of operation is initiated upon loading the memory data table starting address (OUT S' = 4) and range (OUT S' = 5) parameter words into the interface buffer. No response, other than ECHO, is returned to the Hiway.

Listen Only Mode

The listen only mode of operation is initiated with ACT S' = 1. Prior conditioning of the memory data table starting address and range parameter words is required (same as for normal attention mode). No response is returned to the Hiway.

13.2.3 Computer Instructions

The TDC 4500 or HS4400 computer program controls and monitors the operation of the interface by executing GEN 2 instructions addressed to it. The DHI uses a single GENIE Bus address and two non-inhibitable interrupts. Except for test purposes and initial conditioning, all data and command words are transferred directly to and from computer memory through the direct memory access feature of the GENIE Bus. The following is a list of the micro-coded GEN 2 instructions and how they affect the Data Hiway Interface.

ACT S' = 0 - Activates the interface. Must be used after power-up, or following an abort command.

ACT S' = 1 - Selects the listen only mode of operation. No response is returned to the Hiway following reception of unsolicitated data in the attention mode.

ACT S' = 2 - Selects off-line loopback test mode. Must be preceded by ABT S' = 0.

ACT S' = 4 - Generates an interrupt, if required by software, for program linkage or off-line tests.

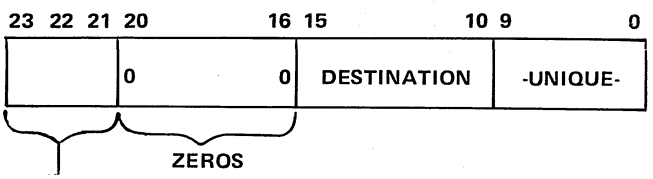
ACT S' = 5 - Selects the back-up Hiway.

ACT S' = 6 - Activate Interrupt Mask (see 4.5.2).

ACT S' = 7 - Deactivate Interrupt Mask (see 4.5.2). Note interface "initialize" will unmask all interrupts.

OPR S' = 7 - Operate preferred access (block transfer or call-up). Transfers the command word from the A Register to the interface and initiates a single Hiway transaction in the preferred access mode of operation. This instruction is issued after the memory table starting address and range parameters have been loaded (see OUT S' = 2, 3). The OUT instructions may be executed in any order and the buffer may be reloaded prior to the OPR, providing the interface is not already busy.

A Register format:



FUNCTION CODE:
BLOCK READ = 111
BLOCK WRITE = 011
CALL UP = 100

Content of the Unique and Destination Fields depends on the device being commanded.

ABT S' = 0 - Abort. Terminates the operation and initializes the interface, including the buffer and the Hiway switch which reverts to prime Hiway.

OUT S' = 1, 2, 3 - Load buffer parameters (preferred access mode). Transfers command memory table (1), data memory table (2), and range (3) parameters from the A Register to the interface buffer (see Fig. 13-6 for A Register formats). The range and data memory table words must precede the command memory table word.

OUT S' = 4, 5 - Load buffer parameters (attention mode). Transfers data memory table (4) and range (5) parameters from the A Register to the interface buffer (see Fig. 13-6 for A Register formats). These instructions can be issued at any time, providing the interface is not already busy.

IN S' = 0 - Input Hiway word. This instruction can be used anytime for test purposes. Upon execution, the last Hiway word sent to or received by the interface, via the DMA function, is transferred to the A Register. See Figs. 13-2 through 13-5 for data word formats.

IN S' = 1 - Input CMD buffer word (preferred access). This instruction can be used anytime for test and error recovery. Upon execution, the current memory address in the interface command buffer is transferred to the A Register. The A Register format is the same as for OUT S' = 1 (see Fig. 13-6).

IN S' = 2 - Input data buffer word (preferred access). This instruction can be used at any time for test and error recovery. Upon execution, the current memory address in

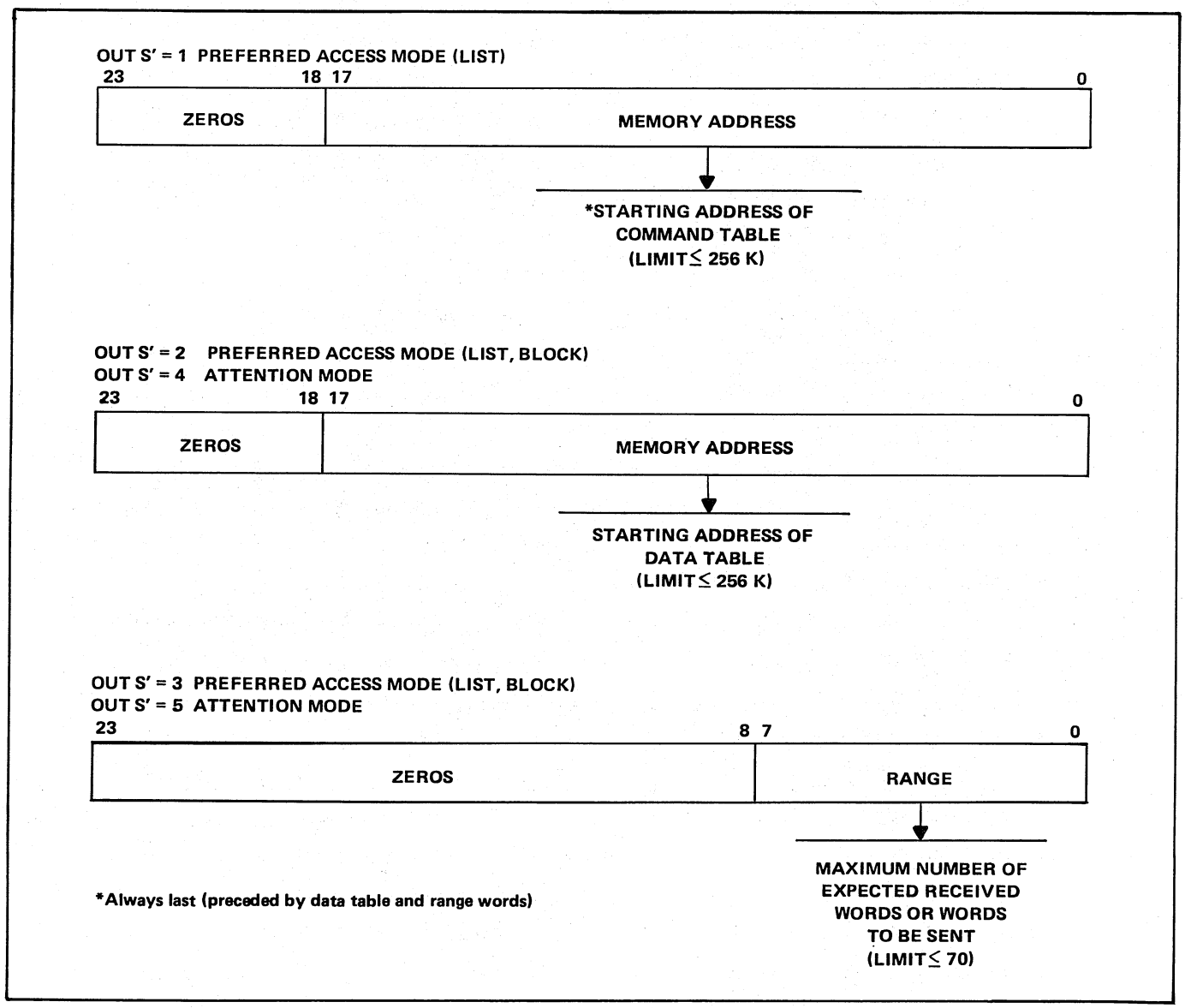


Fig. 13-6 A Register Format - Output Memory Table and Range Parameters

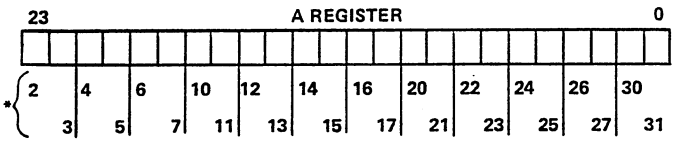
the interface data buffer is transferred to the A Register. The A Register format is the same as for OUT S' = 2 (see Fig. 13-6).

IN S' = 3 - Input range and error status word (preferred access). This instruction can be used at any time for test and error recovery; however, the error status is only updated just before a preferred access interrupt. See Fig. 13-7 for A Register format and error conditions (Preferred Access).

IN S' = 4 - Input data buffer word (attention). This instruction can be used anytime for test and error recovery purposes. Upon execution, the current attention buffer address word is transferred from the interface to the computer A Register. The A Register format is the same as for OUT S' = 4 (see Fig. 13-6).

IN S' = 5 - Input range and error status word (attention). This instruction can be used at any time for test and error recovery purposes; however, the error status is only updated just before an attention interrupt. Upon execution, the current range value and error status, if any, is transferred from the interface to the computer A Register. See Fig. 13-7 for A Register format and error conditions (attention mode).

IN S' = 6 - Input poll response. Transfers the poll response information from the interface to the computer A Register for program interrogation. Any Hiway devices responding to the previous poll, generated by the interface, causes a "one" to be entered into the A Register bit position which corresponds to its octal address. The A Register format is illustrated as follows.

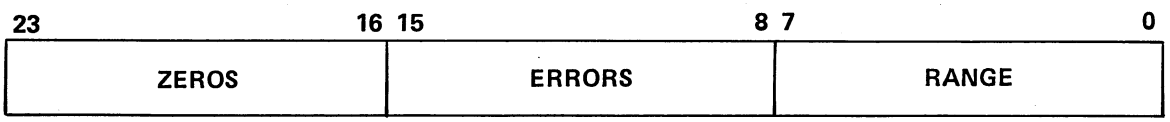


*DEVICE OCTAL ADDRESS

IN S' = 7 - Input block/single commands. Transfers the block/single command information from the interface to the A Register. See OPR S' = 7 for A Register format.

JNR S' = 0 - Jump if not ready. This instruction can be used at any time to test the ready/not ready status of the interface.

JNR S' = 6 - Jump if external HTD in use. This instruction may be used at any time to allow the program to determine whether the interface is or is not allowed to do limited HTD functions.



ERRORS BIT NO.	TYPE (Preferred Access)	TYPE (Attention)
8	BCH ERROR	BCH ERROR
9	BUSY RESPONSE	NOT USED
10	NO RESPONSE	NO RESPONSE
11	USER ERROR	NOT USED
12	ECHO ERROR	NOT USED
13	ILLEGAL RESPONSE	ILLEGAL RESPONSE
14	BLOCK READ RANGE OVERFLOW	RANGE OVERFLOW
15	LIST OPERATION (STATUS ONLY)	LIST OPERATION (STATUS ONLY)

NOTE: The error status portion is cleared whenever a new range is loaded.

Fig. 13-7 A Register Format - Input Range and Error Status

JNE S' = 0 - Jump if no preferred access error. This instruction can be used at any time following a type "0" interrupt to determine the cause of the interrupt. This interface error status bit is cleared by ABT, power-up, OUT S' = 1, or OPR S' = 7.

JNE S' = 2 - Jump if no Hiway access error. This instruction can be used at any time following a type "0" interrupt to determine the cause of the interrupt. This interface error/status bit is cleared by ABT, power-up, OUT S' = 1 or OPR S' = 7.

JNE S' = 4 - Jump if no attention error. This instruction can be used at any time following a type "1" interrupt to determine the cause of the interrupt. If it was caused by an error or alarm condition, program control is transferred to P+1. This interface status bit is cleared by power-up, ABT, or OUT S' = 4.

JNE S' = 6 - Jump if not prime Hiway. This instruction can be used at any time to determine if the back-up or prime Hiway is currently in use. If operation is on the prime Hiway, program control is transferred to P+1.

13.2.4 Error Checks

The error checks performed by the interface are listed on Fig. 13-7. Here is a brief description of each type of error check:

- BCH Error - Each Hiway word contains a BCH check segment in the final five bits. This segment is generated by the source device and checked by the destination device(s). If the interface detects a BCH error, it sets an error bit in the status word, stops the operation and generates a type 1 interrupt.

- Busy Response - Should the interface receive a busy word while waiting for a COMMAND READ response, it will set an error bit in the status word, stop the operation and generate a type 1 interrupt. Not all Hiway devices are capable of returning a busy word.

- No Response - The interface sets a response timer when it expects to receive a response. If the expected response is not completed within 180 usec., EOW received, it sets the error bit in the status word, stops the operation and generates the appropriate interrupt.

- User Error - Should the interface receive an unexpected or out of sequence response, from either the Hiway or the computer, it sets an error bit in the status word, stops the operation and generates the appropriate interrupt.

- ECHO Error - When the interface transmits word data (list) or the last word of a block, the destination device returns the unaltered word for verification. If the 16-bit data field is good, the list will continue, if not, the status bit is set, the operation stops and the appropriate interrupt is generated.

- Illegal Response - A number of tests are made to determine that both Hiway and computer responses are correct for a particular Hiway transaction. For example: tests are made for good source, proper function code, OPR command (if block), and proper address.

  An illegal response will set an error bit in the status word, stop the operation, and generate the appropriate interrupt.

- Block Read Range Overflow - This error occurs anytime the interface receives more data than it was allowed space for. The range register is decremented and reloaded for each Hiway transaction. An overflow will set an error bit in the status word, stop the operation and generate the appropriate interrupt.

13.2.5 Options and Features

The interface meets the environmental specifications of the host computer: Class A General Industrial (0° to 50° C 5% to 95% RH).

The optional application parameters, implemented by switches and jumpers on the interface control PWA, are described as follows:

- GENIE Bus address range = 400_8 - 777_8 (switch selectable)

- Data Hiway address range = 00_8 - 77_8 (switch selectable)

- GENIE Bus priority (1-16) = 33_8 - 77_8 (switch selectable)

- Limited HTD function (POLL). Allows computer based applications with or without the Hiway Traffic Director (jumper selected).

- Source check (switch selectable). Source check can be disabled to accommodate Hiway devices which do not normally respond with a source field (device address).

13.3 PARALLEL DATA LINK

The APDL1 Parallel Data Link (PDL) provides an interface with the same unit in another 4500 system, with a similar unit in another 4000 series process computer, or it interfaces with a 3010 or 3010/2 system via an AE86 High Speed Data Link. In 4050, 4060, 4020, and 4010 systems, the PDL interfaces with an 090/190 Computer Interface Unit (CIU) in the I/O buffer (model 4820BS12 in 4010 systems). The PDL's interface with the opposite computer consists of transformer coupled line drivers and receivers. Characters are transferred in bit-parallel form, and subsequent characters are transferred only after the receiving computer has acknowledged receipt of the preceding character. The two cables connecting the PDL to the opposite computer may be up to 250 feet in length.

13.3.1 Data Format

While data may be transferred through the PDL by means of GEN 2 instructions IN and OUT, TIM/TOM is the principal means of data transfer. When communicating with another APDL1 or with an 090/190 CIU in another 4000 series machine, data are transferred from the 12 least significant bits of the A Register in the transmitting computer to the 12 least significant bits of the A Register in the receiving computer. Each 12-bit data segment is referred to as one half-word. Eight bit bytes are exchanged when communicating with a 3010 or 3010/2 system. When using TIM/TOM to communicate with another computer up to 55,000 halfwords per second may be transferred in one direction. This data link is a full-duplex link - data can be moving in both directions simultaneously, if the program permits.

13.3.2 PDL Instructions

The following GEN 2 instructions affect the PDL transmitter: JCB, JDR, OPR, and OUT. JCB, JDR, IN and OPR affect the receiver. These instructions are defined under 4.5.2 and in Appendix C. OPR has the following special functions:

OPR addressed to the transmitter initiates a PDL operation and transfers a count byte to the PDL, from the eight least significant bits of the A Register. Bits 6 through 0 contain a number equal to the number of half-words in the next record, less one. For example, if the next record is to consist of 128 half-words, bits 6 - 0 will contain $177_8 = 127_{10}$. When the next record is the last record in a file, bit 7 of the transfer count word is set.

OPR addressed to the receiver attempts to activate the receiver and thereby determines if the last half-word in a file has been received. If OPR is successful in setting the receiver busy, either the first half-word in a new record has been received, or the receiver channel has been initialized. Receipt of the last half-word in a file inhibits OPR from setting the receiver busy.

13.3.3 Additional Features

Device Addresses and API's: The PDL uses two GENIE Bus device addresses (transmitter and receiver) and generates four API's (two data exchange and two end-of-record).

Environmental Class: A. (See 3.1.)

13.4 TRANSPARENT SYNCHRONOUS DATA LINK

The Transparent Synchronous Data Link (TSDL) provides communications through data sets and telephone lines or other communications media, or it communicates via a directly connected, transformer coupled interface. The TSDL communicates over a bit-serial syschronous character half-duplex or full-duplex channel to the opposite computer or data terminal. Messages transmitted and received over this data link may utilize ASCII or EBCDIC codes, and the text of such messages may utilize these codes or may be transferred in a transparent mode as binary data or any code agreed upon by the 4500 system and the opposite computer or terminal. This data link is compatible with the IBM Binary Synchronous Communications (BSC) discipline. Message characters are exchanged directly with main memory via the direct memory access feature of the GENIE I/O Bus.

13.4.1 TSDL Interfaces

The TSDL occupies two board slots on the GENIE I/O Bus. Three serial communications interfaces are available as defined by the TSDL model number:

- Model ASDL1, Transformer Coupled Interface. Provides a dc isolated interface to another TSDL or equivalent in the opposite computer or terminal, over a directly connected cable up to 2500 feet in length. This interface operates at up to 240,000 baud.

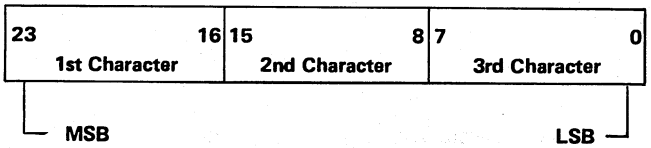
- Model ASDL2, EIA RS232C Interface. Connects a data set or other EIA RS232 interface through up to 50 feet of cable. This interface operates at up to 19,200 baud. May be directly connected to another TSDL via up to 50 feet of cable.

- Model ASDL3, Wide-Band Current Interface. Connects to Bell 303 data set with wide-band current interface, or equal, via up to 50 feet of cable. This interface operates at up to 230,400 baud.

13.4.2 Data Format

The TSDL exchanges 8-bit message bytes directly with main memory via the GENIE I/O Bus. Prior to initiating a TSDL operation (see 13.4.5 and 13.4.9), the program stores the message or messages to be transmitted in main memory and/or reserves up to 65,535 bytes of main memory (21,845 words) for the storage of received characters. Each character transmitted or received in any format consists of eight bits (one byte). The TSDL transmitter fetches characters to be transmitted from main memory and converts each parallel memory character to an 8-bit serial character for transmission over the serial communications channel. The TSDL receiver accumulates serial received characters and stores them as 8-bit parallel characters in main memory. The TSDL can access any location from 0 to 262,144 words. As each TSDL character is transferred the TSDL accesses the next memory byte to fetch or store the next character (see section 4, 4.5.4).

Each word in main memory from which or into which TSDL data are transferred contains three characters (bytes):



The least significant bit of each transmitted or received character is shifted onto the serial data line first, followed by the remaining seven bits in the character. When the TSDL is in the ASCII mode, the most significant bit in each character is an odd parity bit, which is generated by the TSDL for transmission and checked by the TSDL upon reception. If incorrect parity is detected in a received character, the parity bit stored in memory with the character is set equal to one and the receiver PER status bit is set (see 13.4.5). Normally, the program sets the most significant bit to zero in all ASCII characters to be transmitted, but for test purposes only, the program may force transmission of an incorrect parity bit by setting the most significant bit equal to one. This test condition must be enabled also by setting bit 23 of the A Register while executing the OPR instruction that initiates the transmission.

The following is a typical message format (refer to 13.4.3 for control character definitions):

SOH. . .Header. . .STX. . .Text. . .ETX BCC

The header typically contains terminal addressing or routing information. The test may be any type of information, including EBCDIC characters, ASCII characters, or if in transparent mode, any 8-bit characters. The transmitter and/or receiver is placed in either EBCDIC or ASCII mode prior to initiating a message transfer, but can be switched into or out of transparent mode by characters in the text (see 13.4.3).

13.4.2.1 Transparent Mode

The TSDL transmitter converts to transparent mode when it detects control character DLE immediately followed by STX in the output message. The next two bytes in memory are transparent mode byte count bytes that are placed in the message in memory by the program. The first byte accessed contains the most significant byte and the next contains the least significant byte. These two bytes contain the one's complement of the number of transparent bytes plus 1. These two bytes are not transmitted on the data line. If during the transmission of transparent text, a character resembling DLE is recognized, the TSDL inserts and transmits a hardware generated DLE ahead of the character from memory. When the correct number of transparent bytes have been transmitted, the TSDL inserts and transmits a DLE, expecting the next character to be an end-of-message character or US, which will terminate transparent mode in the opposite receiver. If the expected character is not ETX, ETB, ENQ, or US, it is still transmitted, the DLE bit is set in the transmitter status word (13.4.4), and the transmission terminates (see 13.4.9.1). If the expected character is ETX, ETB, or ENQ, the transmission terminates (13.4.9.1) after that character is sent. If it is US, the TSDL remains ready to transmit another message block and reverts to the initial EBCDIC or ASCII mode.

The receiver switches to transparent mode when it detects DLE immediately followed by STX in the incoming message. The DLE and STX characters are stored in memory and zeros are stored in the next two memory bytes. Reception of transparent data then continues until DLE followed

by an end-of-message or US character is detected. The content of the receiver's range register is then stored in the two memory bytes previously filled with zeros. If the DLE at the end of transparent text is followed by ETX, ETB, or ENQ, message reception terminates as the ETX, ETB, or ENQ character is stored in memory (13.4.9.2). Since the program knows the initial value of the range register and the starting memory address of the data block, it can use the stored value of the range register to determine the length of the transparent data block and its location.

The TSDL transmitter and receiver recognize the following control character pairs in the incoming and outgoing character streams as described:

DLE STX - Start of Transparent Text. Switch to transparent mode as described in the two preceding paragraphs.

DLE ETB - End of Transparent Block. Switch from transparent mode. And end-of-message character (see 13.4.9).

DLE ETX - End of Transparent Text. Switch from transparent mode. An end-of-message character (see 13.4.9).

DLE SYN - Fill characters. Transmitted when a transparent data character is not provided in time to be transmitted in a character slot on the serial data line. Such character pairs are not stored in memory when received by the TSDL receiver.

DLE DLE - Used to confirm the presence of a data character in the transparent data stream that appears to be DLE. The TSDL transmitter automatically inserts the second DLE and the receiver stores only the data DLE in memory.

DLE US - Unit Separator. Indicates the end of a transparent text block, but not the end of a message. The TSDL transmitter remains in the transmit state. The TSDL receiver remains ready to receive another message.

DLE ENQ - Abort Transparent Text. Indicates to the receiving end that the transparent text transmission is being discontinued unexpectedly, and to disregard transparent text already sent in this block. An end-of-message character (see 13.4.9).

DLE EOT - End of Transmission. Not expected to terminate transparent mode, but still functions as an end-of-message character (see 13.4.9).

13.4.2.2 ASCII Data Link Escape Sequences

DLE sequences within the text of both transmitted and received ASCII messages have the following form:

DLE. . .One or More Characters. . . .End

The characters between DLE and the "End" character can be any octal code equal to 100_8 and above. The "End" character can be any octal code from 00_8 to 077_8 and it signifies the end of the DLE sequence. If the "End" character code is from 000_8 through 037_8, its normal control function is recognized, and it is treated as an end-of-message character (see 13.4.9) if that is included in its normal function. If the "End" character code is from 040_8, through 057_8, it is not treated as an end-of-message character. If the "End" character code is from 060_8 through 077_8, it is treated as an end-of-message character.

13.4.3 Character Recognition

The following characters in the transmitted or received message stream are recognized as control characters and the TSDL hardware responds as indicated. The octal character codes recognized in ASCII mode (xxx_8) are followed by the hexadecimal codes recognized in EBCDIC mode (X'xx').

ACK (006_8) Positive Acknowledgement. Indicates to the sender that his message was received and accepted. Treated as an end-of-message character (see 13.4.9) if not within the header or text of a message (see 13.4.2).

DLE (020_8, X'10') Data Link Escape. See 13.4.2.1 Transparent Mode and 13.4.2.2 ASCII Data Link Escape Sequences. Also see the "Stick Characters" paragraph under this Character Recognition heading.

ENQ (005_8, X'2D') Enquiry. May be used as a request for a response from a remote terminal or in a DLE ENQ character pair to abort transparent mode (13.4.2.1). Treated as an end-of-message character.

EOT (004_8), X'37') End of Transmission. Indicates the end of a transmission containing one or more blocks of text and associated headings. Treated as an end-of-message character when not in the heading or text of a message.

ETB (027_8, X'26') End of Transmission Block. Indicates the end of a data block. Treated as an end-of-message character.

ETX (003_8, X'03') End of Text. Terminates a text character sequence started with STX. Treated as an end-of-message character.

NAK (25_8, X'3D') Negative Acknowledgement. Indicates to the sender that his message was not accepted. Treated as an end-of-message character if not within the header or text of a message.

SOH (001_8, X'01') Start of Header. Indicates that the characters to follow are the message header. EOT, NAK, and ACK are not treated as end-of-message characters if they follow SOH in the same message block.

STX (002_8, X'02') Start of Text. Indicates that the characters to follow are text characters. EOR, NAK, and ACK are not treated as end-of-message characters if they follow STX in the same message block.

SYN (026_8, X'32') Synchronous Idle. Use to synchronize the receiver with the transmitter in a synchronous serial data link. The TSDL transmitter transmits at least three hardware generated SYN's prior to each message and the receiver requires at least two SYN's to achieve synchronization. The transmitter transmits a SYN, should a character not be available from memory in time for transmission. The receiver discards all received SYN's and does not store them in memory.

US (37_8, X'IF') Unit Separator. Indicates the end of a message block but is not treated as an end-of-message character, i.e., other message blocks may follow. Also see the DLE US description under 13.4.2.1.

Stick Characters. The so called "stick" characters are certain characters following DLE. They are treated as end-of-message characters. In EBCDIC mode, they are DLE followed by one of the following hexadecimal codes: 61, 62, 64, 67, 86, 6B, 6D, 6E, 70, 73, 75, 76, 79, 7A, and 7C. In ASCII mode, they are DLE followed by an octal code from 060 through 077. The following "stick" characters may be defined by the software and/or the opposite computer or terminal as indicated:

DLE 60_8 or DLE X'70'	=	ACK0 or Positive Acknowledge 0.
DLE 61_8 or DLE X'71'	=	ACK1 or Positive Acknowledge 1.
DLE 73_8 or DLE X'6B'	=	WACK or Wait Before Transmitting/Positive Acknowledgement.
DLE 74_8 or DLE X'7C'	=	Reverse Interrupt (a form of positive acknowledge).

13.4.4 Message Validity Verification

When the program issues an OPR instruction to the TSDL transmitter or receiver to initiate a message transfer (13.4.5) it specifies one of two types of message validity verification. For ASCII messages, the program may specify the checking or generation of a 2-byte polynomial check segment derived from the text using the polynomial $X^{16} + X^{15} + X^2 + 1$, or it may specify a 1-byte longitudinal checksum character. For EBCDIC messages, the 2-byte check segment, only, is used. These check segments and longitudinal checksum characters are often referred to as "BCC" - Block Check Code Characters. The BCC is accumulated by the transmitter as messages are transmitted and transmits the BCC immediately after the ETB, ETX, or US character in the message, which defines the end of the text block. The receiver accumulates the BCC as messages are received and it compares the BCC received immediately following ETB, ETX, or US with the accumulated BCC, and stores zeros in the one or two bytes in memory immediately following the location where it stored ETB, ETX, or US if the received BCC is identical to the accumulated BCC. If the BCC does not compare, a non-zero residue in stored in the one or two BCC bytes in memory.

The program normally stores zeros in the one or two bytes immediately following ETB, ETX, or US in messages to be transmitted to specify that a true BCC is to be transmitted. For test purposes, the program may store non-zero codes in the one or two BCC bytes to cause the transmitter to transmit a modified BCC. This test feature must also be enabled by setting bit 23 of the A Register while the OPR instruction is executed to initiate the message transmission.

13.4.4.1 Check Segment Accumulation

For both transmission and reception, the accumulation of the polynomial check segment begins with the character following SOH, or if STX is encountered first in the message stream, accumulation begins with the character following STX. The accumulation continues through the last character in the message block, which will be ETB, ETX, or US. The only characters excluded from the accumulation are SYN, DLE SYN character-pairs, the first DLE of a DLE DLE pair in transparent mode, and the DLE of DLE ETB, DLE ETX, or DLE US character-pairs. If the message block ends with US, the accumulation is reset and restarted with the first character of the next message block. The first character follows the BCC of the preceding block and the SYN characters between blocks.

13.4.4.2 Longitudinal Checksum Accumulation

For both transmission and reception, the accumulation of the longitudinal checksum begins with the first character after the first STX or SOH character in the message block. All characters thereafter with the exception of SYN are included, and the accumulation continues through the last character in the message block, which will be ETB, ETX, or US. If the message block ends with US, the accumulation is reset and restarted with the first STX or SOH in the next message block.

13.4.5 TSDL Instructions

The program controls and monitors the operations of the TSDL by executing GEN 2 instructions addressed to the transmitter and to the receiver. Except for test purposes, the program does not transfer transmitted or received data throught the TSDL. Normal data transfers are made through the direct memory access feature of the GENIE I/O Bus. Refer to section 4; 4.5.2 for a description of the instruction formats and operation. The specific functions of the instructions as applied to the TSDL are described in the following. The symbol "Tx" indicates an instruction addressed to the TSDL transmitter and "Rx" indicates an instruction addressed to the TSDL receiver.

ACT S' = 0 (Tx) = Turn On Data Terminal Ready (DTR) at data set interface. DTR indicates to the data set or the opposite computer or data terminal that the TSDL and the computer are present with power applied. When using a dial-type phone network, DTR has the effect of "taking the phone off the hook". If DTR is turned off for more than approximately one-half second, the line typically disconnects. With private or leased lines that are permanently connected, DTR is normally left on continually.

ACT S' = 1 (Tx) = Turn-Off Data Terminal Ready (DTR).

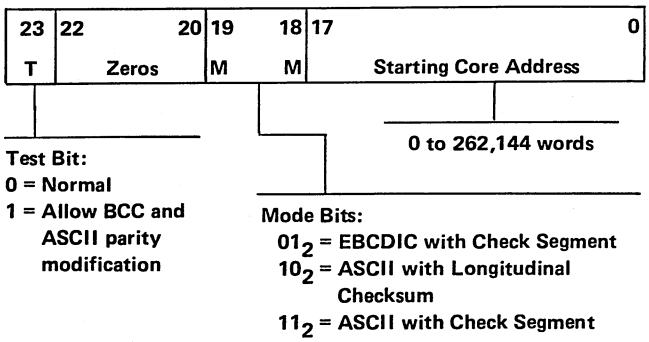
ACT S' = 2 (Tx or Rx) = Generate end-of-message API. Normally used only for test purposes.

ACT S' = 3 (Tx) = Generate Ring API. Normally used only for test purposes.

ACT S' = 6 (Rx or Tx) = AIM - Activate Interrupt Mask (see 4.5.2).

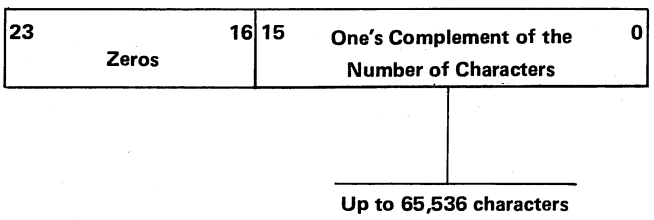
ACT S' = 7 (Rx or Tx) = DIM - Deactivate Interrupt Mask (see 4.5.2). Test programs may use this instruction to inhibit memory requests by issuing it to Tx after activating Tx with an OPR executed while bit 23 of the A Register is set.

OPR S' = 0 (Rx or Tx) = Initiate a message transfer. When issued to Tx, this instruction causes the Request to Send (RTS) signal at the data set interface to go true. Transmission cannot begin until Clear to Send (CTS) goes true in response to RTS. CTS goes true when the communication line is established, or after a sufficient delay to allow it to be established. The content of the A Register when OPR S' = 0 is executed specifies the operation mode as follows:



After any message transfer in progress is completed, OPR S' = 0 initializes all of the TSDL except for the DTR line to the data set interface and error indications. ABT must precede OPR S' = 0 to reset error indications prior to a new message transfer. Since the TSDL does not check parity on the transfer from the A Register, it is good practice to verify the contents of the address register with IN S' = 2.

OPR S' = 1 (Rx) = Load the receiver range register. The TSDL does not check parity on the data transferred from the A Register, so it is good practice to verify a correct transfer with IN S' = 2. OPR S' = 1 should be issued to the receiver before OPR S' = 0 or OPR S' = 2 so that IN S' = 2 can be used to verify a correct range register transfer. The content of the A Register while OPR S' = 1 is executed indicates the number of characters to be stored in memory as the next message is received:



OPR S' = 2 (Tx or Rx) = Initiate a test mode transfer. See OUT S' = 0 and IN S' = 0. The A Register contents when OPR S' = 2 is executed have the same meaning as for OPR S' = 0. OPR S' = 2 is used only by test and diagnostic programs.

ABT S' = 0 (Tx or Rx) = Abort. Initializes the TSDL except that the DTR line to the data set interface is unaffected.

OUT S' = 0 (Rx) = Output test data bits. OUT S' = 0 transfers the content of the least significant bit of the A Register to the TSDL receiver just as if it was an incoming bit on the received data line. The assembled characters are stored in main memory as in normal operations. Such a transfer must be initiated by OPR S' = 2 issued to the receiver.

IN S' = 0 (Tx) = Input test data bits. IN S' = 0 transfers a transmitter data bit to the least significant bit of the AU's A Register, just as if it was being shifted onto the transmitted data line. The test message characters are fetched from main memory as in normal operations. Such a transfer must be initiated by OPR S' = 2 issued to the transmitter.

IN S' = 1 (Tx or Rx) = Input TSDL status. IN S' = 1 transfers the status of the transmitter or receiver to the A Register and may be executed at any time with no effect on the TSDL operation. The status words are:

Receiver;

23 12	11	10	9	8	7	6	5	4	3	2	1	0
Zeros	TXT	TSP	RCV	CBY	CON	EOR	OVF	CDE	PER	BCE	DLE	BPE

Transmitter;

23 8	7	6	5	4	3	2	1	0
Zeros	TSP	RNG	CTS	DSR	RTS	DTR	DLE	BPE

The status bits have the following meanings:

TSP; Tx or Rx is in transparent mode.

RNG; A ring signal is being received from the data set interface. This bit can go true only while DTR to the data set interface is off.

CTS; Clear to Send at the data set interface is true.

DSR; Data Set Ready at the data set interface is true.

RTS; Request to Send from the TSDL to the data set interface is true.

DTR; Data Terminal Ready from the TSDL to the data set interface is true.

DLE; An invalid DLE character sequence has been detected. See 13.4.2.1.

BPE; A GENIE I/O Bus data parity error has been detected. See 4.5.5.

TXT; SOH and/or STX have been detected in an incoming message block, so the receiver is in the text or header mode.

RCV; The receiver is accumulating incoming SYN or message characters after having been initiated by OPR S' = 0 or S' = 2.

CBY; OPR S' = 0 or S' = 2 has been issued to the receiver and no end-of-message character has yet been detected, therefore the receiver channel is busy.

CON; Carrier On. The data set has detected the carrier from the distant data set. In directly connected EIA RS232 interfaces, this line is connected to RTS from the opposite computer or terminal.

EOR; End of Range Register. The range register is full so the receiver can transfer no more characters to main memory.

OVF; Overflow. A received character was replaced by a new incoming character before it could be stored in main memory. This sets the receiver channel not busy.

CDE; Carrier Drop-Out Error. The CON bit went false while receiving a message. This carrier fade-out can be caused by a temporary signal fade or noise in the telephone or communications system. This bit sets when carrier detect line at the data set interface goes false while the receiver channel is busy and a message is being received.

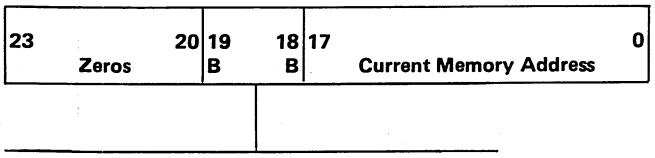
PER; Parity Error. A parity error was detected on an incoming ASCII character. The most significant bit in each such character is set as it is stored in main memory.

BCE; Block Check Error. A 2-byte check segment or 1-byte longitudinal checksum comparison error was detected on an incoming message block. The BCC character or characters in memory for such message blocks will be non-zero.

IN S' - 2 (Tx or Rx). This instruction when issued after OPR S' = 0 or S' = 2 to the same channel, transfers the content of the channel's address register to the A Register. When IN S' = 2 is issued to the receiver immediately following OPR S' = 1, but prior to OPR S' = 0 or S' = 2, the content of the range register is transferred to the A Register.

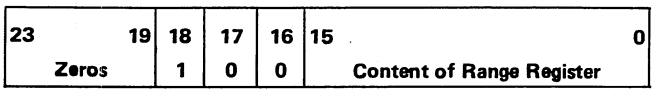
The address register and range register words have the following formats:

Address register;



01_2 = Next character to or from M.S. byte
10_2 = Next character to or from middle byte
11_2 = Next character to or from L.S. byte

Range register;



JCB S' = 2 (Tx or Rx). Jump if channel busy. See 4.5.2.

JNE S' = 0 (Tx or Rx). See 4.5.2. No jump if any of the following status bits is set: DLE, BPE, OVF, CDE, PER, or BCE.

13.4.6 Interrupts

The TSDL transmitter generates two interrupts. The type 0 API request occurs when a ring signal is detected at the data set interface. The type 1 API request occurs when an end-of-message character is detected in the output message stream and the transmitter has dropped the request to send signal to the data set interface.

The TSDL receiver generates one interrupt only, a type 1 API request which is generated when an end-of-message character is stored in main memory or when the OVF receiver status bit sets, indicating that the range register is full, yet characters continue to be received on the received data line. The receiver channel will be not busy after an end-of-message character is stored but it will remain busy if an incoming message exceeds the number of characters specified by the range register.

13.4.7 Automatic Answering

When a ring signal is received on the data set interface, the TSDL transmitter generates its type 0 API, which indicates to the program that a call is incoming. The program responds by initiating a received message transfer. The ring signal can be received only when DTR from the TSDL is false. If it is true, the calling station will get a busy signal, just as if the phone was off the hook.

13.4.8 Line Turnaround

Line turnaround is necessary when two-way half-duplex communication is used. In such data links, the transmitter is typically allowed to turn on its RTS line when the received carrier is off, as indicated by the CON receiver status bit. An ACT S' = 0 instruction issued to the transmitter turns on the RTS signal to the data set interface, and transmission may commence (after OPR S' = 0 is issued) when CTS is received from the interface, as the line is turned around. RTS is turned off by the TSDL when the final character in a message is transmitted plus a PAD (all ones) character. This typically drops the received carrier at the other end, allowing it to turn the line around once again. The length of time required to turn the line around is indicated by the interval from RTS to CTS, and with two-wire communications lines may be several milliseconds. Turnaround time can be reduced considerably or eliminated if four-wire lines are used.

13.4.9 Operating Sequences

The following are summaries of the TSDL operating sequences. Details of these operations are provided in the preceding paragraphs. Two-way half-duplex operation with line turnaround is assumed in these sequences, but with a directly connected interface or with full-duplex data sets and phone lines, both the transmitting sequence and the receiving sequence can occur simultaneously.

13.4.9.1 Transmitting Sequence

1. The program stores the message characters in main memory.

2. If Data Terminal Ready has not been left on from some previous operation, the program issues ACT S' = 0 to the transmitter to turn on DTR at the data set interface.

3. When it is legal for the TSDL to begin transmitting (normally, when the received carrier detect signal at the data set interface goes false as indicated by receiver status bit CON), the program issues OPR S' = 0 to specify the transmitting mode and to indicate the starting address in memory. This causes the TSDL to raise Request to Send at the data set interface. RTS normally raises the data set's transmitted carrier.

4. When the connection to the opposite computer or data terminal has been established, Clear to Send from the data set interface goes true, the transmitter transmits three SYN characters, begins to fetch message characters from main memory, and transmits them.

5. When the transmitter recognizes an ETB, ETX, or US character in the outgoing message, it transmits the appropriate Block Check Code in the next character slot or the next two character slots.

6. When the transmitter recognizes an end-of-message character (ETB, ETX, ENQ, or a DLE Stick character-pair, as well as ACK, NAK, and EOT when not in the header or text of a message), the transmitter transmits a PAD (all one's) character, drops RTS and generates an end-of-message API.

13.4.9.2 Receiving Sequence

1. The program reserves a message block of up to 65,536 characters (21,845 words plus one character).

2. If Data Terminal Ready has not been left on from some previous operation, the program issues ACT S' = 0 to the transmitter to turn on DTR at the data set interface.

3. The program issues OPR S' = 1 to the receiver to load the receiver range register with the character count and then executes IN S' = 2 to verify that the count was loaded correctly.

4. The program issues OPR S' = 0 to the receiver to initiate message reception and to specify the starting memory address of the received message block.

5. When the received carrier detect signal from the data set interface comes on (as indicated by receiver status bit CON) serial character reception can begin. When the receiver has become synchronized by the reception of at least two SYN characters, it begins storing message characters in memory.

6. When the receiver detects ETB, ETX, or US in the incoming message stream it checks the BCC which follows and stores the residue in the next character or the next two characters in memory. The residue bytes will contain zeros if no error is detected and will be non-zero if an error is detected.

7. When the receiver detects an end-of-message character (ETB, ETX, ENQ, or a DLE Stick character-pair, as well as ACK, NAK, and EOT when not in the header or text of a message). it generates an end-of-message API. The program may then turn the line around to transmit a reply.

13.4.10 Additional Features

Device Addresses and API's: The TSDL uses two GENIE Bus device addresses (transmitter and receiver) and generates three API's (see 13.4.6).

Environmental Class: A. (See 3.1.)

13.5 HS7024 COMMUNICATIONS COUPLER

The AXTC1 HS7024 Communications Coupler (HCC) provides communications through data sets and telephone lines or other communications media with Honeywell Series 7024 Telecontrol Equipment Remote Stations. The HCC communicates over a bit-serial, half-duplex channel to the remote station(s). Up to 29 remote stations may be connected to the same channel on a party line basis. Either two-wire lines or four-wire lines may be used. Four-wire lines minimize the time needed to change the direction of transmission, especially when used to communicate with a single remote station.

Messages transmitted by the HCC consist of a single 16-bit half-word or a single 32-bit full-word. For most half-word or full-word commands transmitted by the HCC, a reply is expected from the addressed remote station. The remote station's reply may be only a single 16-bit half-word or it may be a combination of half-words and several full-words, with no time interval between the words in the message. Every transmitted and received half-word and full-word begins with a start bit (space, equal to 0), and the final five bits in each half-word or full-word are a Bose-Chauduri (BCH) polynomial check code, which is generated and checked by the hardware to detect transmission errors that may occur on the communications channel.

The message sequences, command definitions, transmitted codes, and data formats used on the HS7024 communications channels are defined in detail in the HS7024 Telecontrol Equipment Summary Manual, PTH-011.

13.5.1 HCC Interfaces

The HCC occupies a single slot on the GENIE I/O Bus and its received data is stored directly in main memory. The data set (modem) interface complies with EIA standard RS232C. A wide variety of data sets may be used, provided the data sets at the computer and remote station sites are compatible. Suitable data sets are:

- Honeywell Model AH402; Asynchronous, 1200 or 1800 Baud. This data set is compatible with the optional 1612K90G13 built-in modem in the remote stations.

- Honeywell Model AH401; Asynchronous, 75 to 300 Baud.

The HCC operates at the following baud rates (baud = bits per second): 75, 110, 150, 200, 300, 600, 900, 1200, 1800, 2400, 4800, and 9600. The transmitting and receiving baud rate clocks are generated in the HCC and it supplies a transmitted baud rate clock to the data set (RS232C circuit DA). The HCC supports communication channels requiring baud rate accuracy up to $\pm$0.01%. Data sets requiring greater baud rate accuracy are not accommodated.

Private or leased telephone lines or other communications media are normally used. Two-wire lines may be used, but four-wire lines will minimize or eliminate the time needed to turn the lines around to change the direction of transmission.

13.5.2 Command and Data Formats

The program transfers commands to be transmitted by the HCC by placing them in the Arithmetic Unit's A Register and then executing an OPR S' = 0 or 1 instruction addressed to the HCC. Data received in a remote station's reply is stored directly in main memory, so the program must reserve memory space prior to issuing an OPR instruction to transmit the command (13.5.4). Before issuing the OPR instruction, the program must also inform the HCC of the starting memory address for the received data and of the maximum number of words expected in the remote station's reply. The starting address and maximum number of received words are transferred by OUT instructions (see 13.5.4). Certain commands do not cause a remote station reply, and the two OUT instructions need not precede the transfer of such commands.

13.5.2.1 Transmitted Command Words

Fig. 13-8 illustrates the form of 16-bit and 32-bit command words in the A Register and the resulting communications line image after the command is transferred to the HCC by an OPR instruction. Note that in the 32-bit full-word commands, A Register bits 2 through 0 contain zeros, which are inverted by the HCC to be transmitted as one's in compliance with the HS7024 command format. The command formats and expected replies are described in the "Telecontrol Subsystem Operation" section of PTH-011, HS7024 Telecontrol Equipment Summary Manual.

13.5.2.2 Received Data Words

Fig. 13-9 illustrates the form of the 16-bit and 32-bit received data words and the corresponding images stored in main memory by the HCC. Should the HCC detect a BCH check segment error in a received word, the corresponding memory location is filled with ones. Note that in a check-back (CHBK) word, bits 12 through 16 and bits 25 through 27 of the line image from the remote station are ones, and these bits are inverted by the HCC and are stored in the corresponding positions in main memory as zeros. Also note that the remote station address (RS) in the line image is complemented, but the HCC stores RS in memory in its true form. The command formats and expected replies are described in the "Telecontrol Subsystem Operation" section of PTH-011, HS7024 Telecontrol Equipment Summary Manual.

13.5.3 Message Validity Verification

Each transmitted command word and each received data word contains a BCH check segment in the final five bits. The transmitting hardware generates the check segment by accumulating a value from the transmitted "one" bits per the polynomial $X^5 + X^2 + 1$. The receiving hardware in the HCC and the remote stations accumulates such a check segment as each half-word or full-word is received. The accumulated check segment is then compared with the pattern in the final five bits in the incoming word, and if the two patterns do not compare exactly, a transmission error has been detected.

When the HCC detects a check segment error, it places "ones" in every bit position in the main memory location in which the received word would otherwise have been stored. The program can verify correct reception of all words in a remote station reply by addressing a JNE instruction to the HCC. If the JNE indicates an error, the program would then typically examine the data block in memory, and request retransmission of all data in which an error was detected.

When a remote station detects a BCH check segment error in a command word from the computer, it ignores the command word. The program can also detect this situation through a JNE addressed to the HCC, and can verify it by checking the HCC status word time-out bit, RTO. See 13.5.4.

The check segment transmitted by the HCC is in its true form on the communications lines but the check segment transmitted by the remote stations is complemented. This is because each of the remote stations on a two-wire party line "hears" the transmission of the other remote stations.

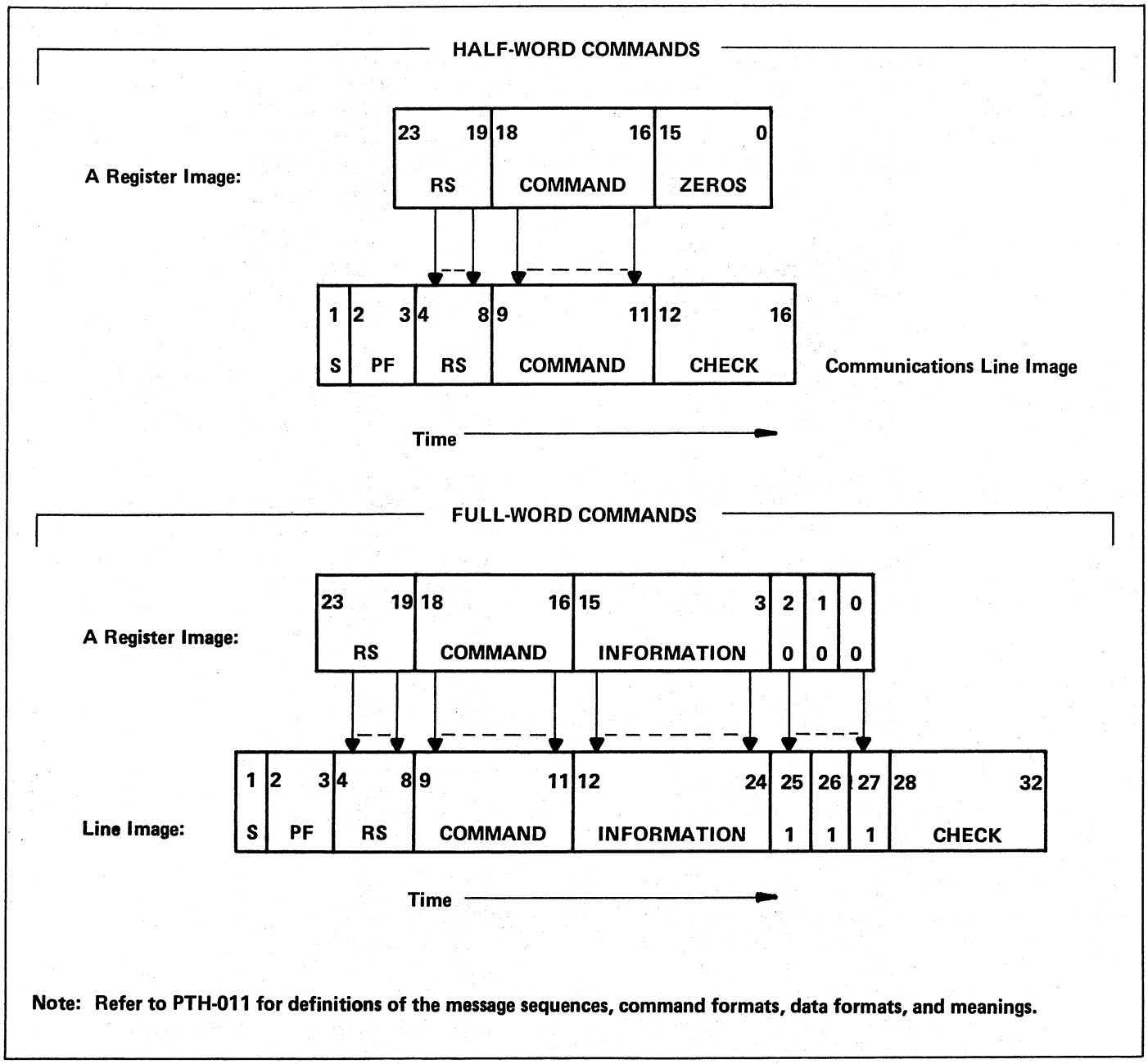
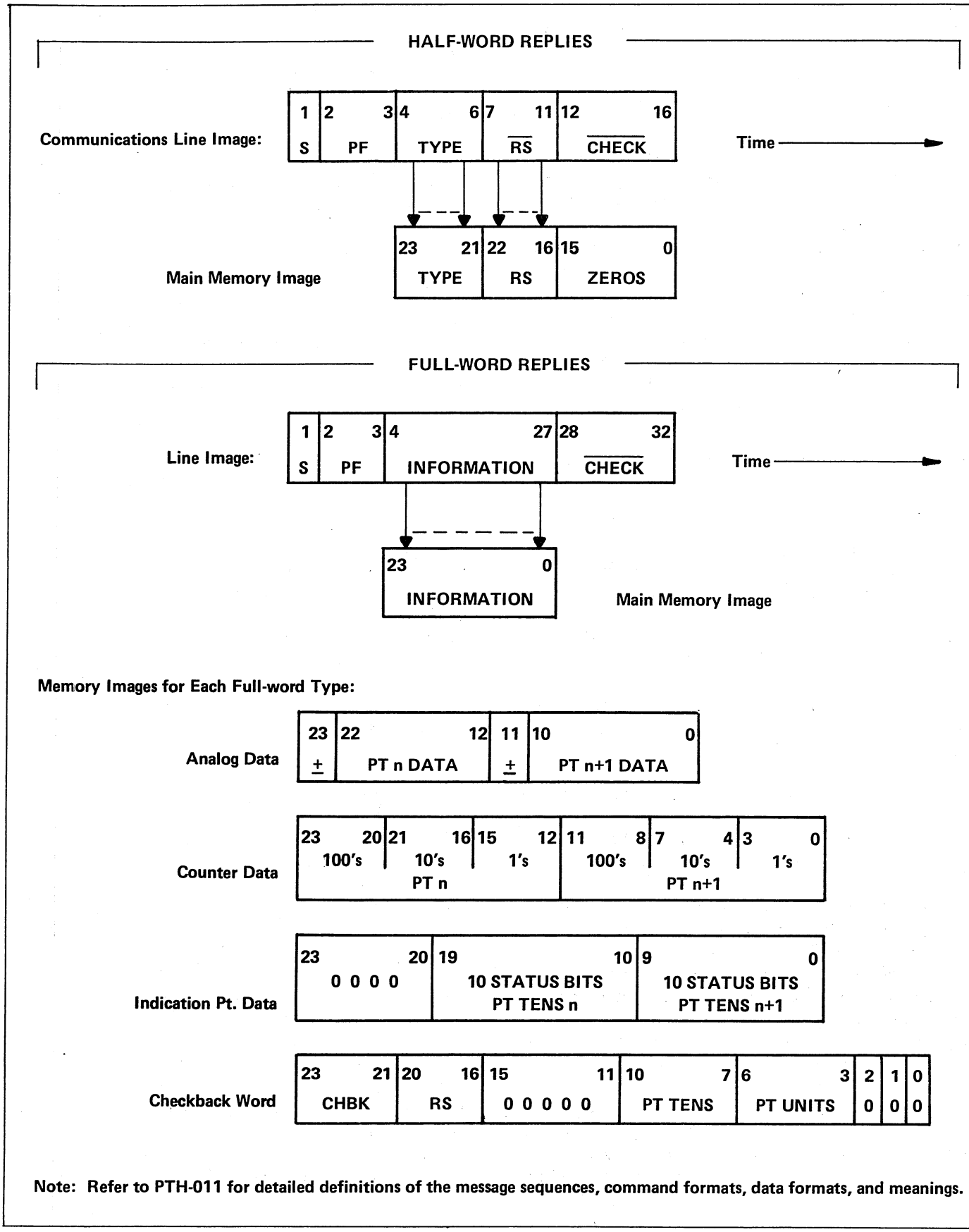


Fig. 13-8 Computer to Remote Station Commands



Note: Refer to PTH-011 for detailed definitions of the message sequences, command formats, data formats, and meanings.

Fig. 13-9 Remote Station Replies

Because the remotes expect a true check segment, they ignore the complemented check segments from other remotes. The HCC hardware inverts the complemented check segments received from the remotes before comparing with the accumulated check segment.

13.5.4 HCC Instructions

The program controls and monitors the HCC operations by executing GEN 2 instructions addressed to it. The HCC uses a single GENIE Bus device address. Except for test purposes, the program does not transfer received data through the HCC. It does transfer transmitted commands through the HCC via OPR instructions, but the received data is stored directly in main memory through the direct memory access feature of the GENIE I/O Bus. Refer to paragraph 4.5.2 in this General Description for a description of the GEN 2 instruction formats and operation. The specific functions of the instructions as they are applied to the HCC are described in the following paragraphs.

ACT S' = 0 = Activate external output signal on data set interface. The external output signal is a special purpose signal provided for special applications. It is not a standard RS232C signal, and has no effect on most data sets. Once turned on, external output remains on until turned off by ACT S' = 1 or the detection of an undervoltage by the power subsystem bus level monitor.

ACT S' = 1 = Terminate the external output signal. Turns external output off (low = false).

ACT S' = 2 = Generate end-of-message API. May be used for test purposes and may be used by software for program linkage.

ACT S' = 6 = Activate Interrupt Mask (see 4.5.2).

ACT S' = 7 = Deactivate Interrupt Mask (see 4.5.2).

OPR S' = 0 = Transfer full-word command. Issued only to the HCC after the range register has been loaded (OUT S' = 3) and the starting memory address for received data has been transferred to the HCC (OUT S' = 1). OPR S' = 0 transfers the command word from the A Register (Fig. 13-8) and the HCC then transmits the command if Clear to Send from the data set interface is true, or when it becomes true.

OPR S' = 1 = Transfer half-word command. For half-word commands to which a remote station reply is expected, the instruction must be preceded by OUT S' = 3 and OUT S' = 1 to load the range register and the starting memory address. Commands RAPT, STRE, and RSET do not cause a remote station reply, so they may be sent without conditioning the HCC to receive data. The command is transmitted if Clear to Send from the data set interface is true, or when it becomes true.

OPR S' = 2 = Set up HCC to receive in remote station role. This instruction is reserved for applications other than the normal application in which the HCC operates as an HS7024 Master Station.

OPR S' = 3 = Set up HCC to transmit in the remote station role. This instruction is reserved for application other than the normal application in which the HCC operates as an HS7024 Master Station.

OPR S' = 4 = Transfer a test full-word. This instruction is used for test purposes, only. The HCC receiver is placed in transparent mode and the full-word contained in the A Register is transferred from the HCC transmitter through a test plug to the receiver. The transmitter adds the start bit, prefix, and check segment and the receiver transfers the full 32 bits as two 16-bit words to the AU A Register (see IN S' = 0).

OPR S' = 5 = Transfer a test half-word. This instruction is used for test purposes, only. The HCC receiver is placed in transparent mode and the half-word contained in the A Register is transferred from the HCC transmitter through a test plug to the receiver. The transmitter adds the start bit, prefix, and check segment and the receiver transfers the full 16 bits to the AU A Register (see IN S' = 0).

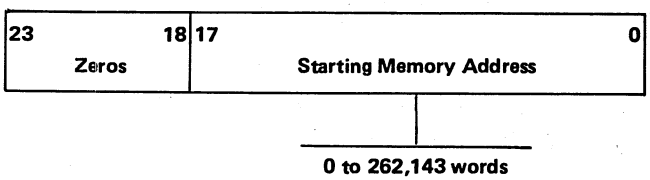
OPR S' = 6 = Test the receiver BCH and stripping logic. Places the transmitter in transparent mode, so that the receiver's BCH check segment checking and bit stripping logic can be checked. This instruction is used for test purposes, only. After the transmitter is placed in transparent mode by this instruction, OUT S' = 0 is used to transfer two 16-bit half-words through the transmitter and a test plug. The receiver places the received data in main memory as indicated by the memory address register and the range register. The test program can alter the start bit, prefix, and check segment patterns to verify correct operation of the receiver.

OPR S' = 7 = Test the transmitter through a transparent receiver. Places the receiver in transparent mode, so that the correct transmission of the start bit, prefix, and BCH check segment by the transmitter can be verified by the test program. After the receiver is placed in transparent mode, the memory word indicated by the address and range registers is fetched from main memory, the start bit, prefix, and BCH check segments are added and transferred to the receiver through the test plug. IN S' = 0 is used to transfer two 16-bit words to the AU A Register for verification by the test program.

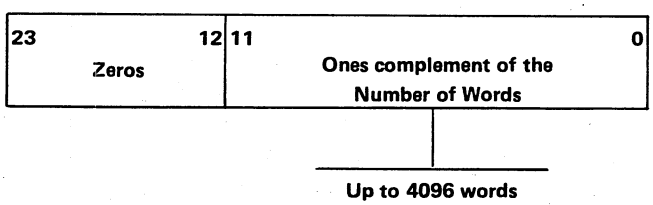
ABT S' = 0 = Abort. Initializes the HCC, clearing out all flip-flops and indicators except the special external output signal (see ACT S' = 0 and S' = 1).

> **NOTE**
>
> To insure that the receive clock is in synchronism with the beginning of a message, an ABORT command must be issued prior to each transmission.

OUT S' = 1 = Load the memory address register. The AU A Register should contain the absolute address of the first word in the memory block which the HCC is to start transferring information from or to memory. The HCC address register is incremented as each word is stored in or read from memory. This instruction should precede an OPR instruction which transfers a command word to which a remote station reply is expected. The memory address register also indicates the location from which a test word is transferred by OPR S' = 7.

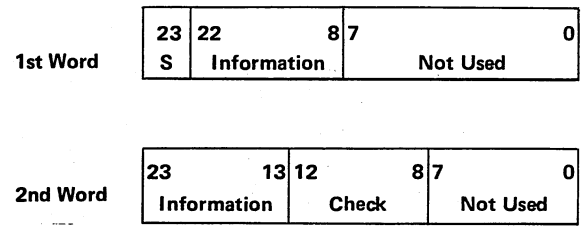


OUT S' = 3 = Load the Range Register. The AU A Register should contain the ones complement of the maximum number of expected received words or the number of transmitted words for test purposes (see OPR S' = 7). For example, if 15_{10} words are to be transferred, the A Register should contain 00007760_8. Since the range register consists of bits 11 through 0, A Register bits 23 through 12 are ignored, and the maximum number of words in a transfer is 4096_{10}. This instruction should precede the transmission of a command word via OPR, to which a remote station reply is expected. A Register format is:

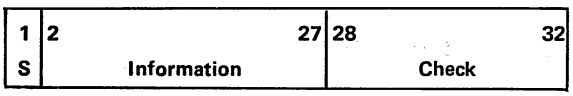


OUT S' = 0 = Output a test half-word to a transparent transmitter. Two of these instructions are used to transfer half-words containing a start bit, prefix, and BCH check codes, from the AU A Register to the HCC transmitter, after it has been placed in transparent mode by an OPR S' = 6 instruction. JDR is used to determine when the HCC is ready to accept each word. This instruction is used for test purposes, only. The data formats are:

A Register Image;



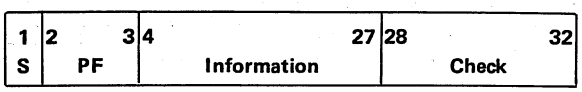
Line Image (via test plug);



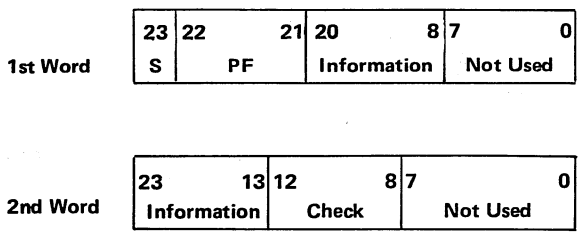
IN S' = 0 = Input data from HCC receiver. This instruction can be used to transfer data received by the HCC to the AU's A Register, rather than storing it directly in main memory. If the receiver is not in transparent mode, the data format is as on Fig. 13-9. If it has been placed in transparent mode by OPR S' = 7, the data format is as follows. JDR is used to determine when the HCC is ready to transfer a word.

Transparent word format:

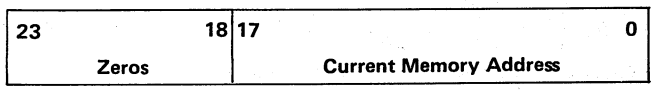
Line image;



A Register Image;



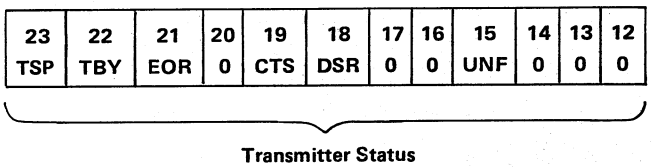
IN S' = 1 = Interrogate address register. Transfers the content of the HCC memory address register to the AU's A Register. This instruction has no other effect and may be executed at any time. The A Register content is:

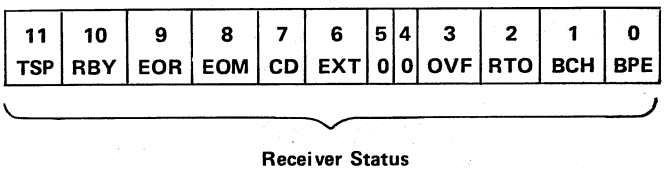


NOTE

Since once started, normal command transmission and data reception by the HCC are not under program control, it is good practice to make sure that the range and address registers have been correctly loaded, by executing IN S' = 3 and IN S' = 1 before issuing the OPR S' = 0 or OPR S' = 1 to initiate the HCC operation.

IN S' = 2 = Input HCC status. Transfers the content of the HCC status register to the AU's A Register and may be executed at any time. If any of the status bits indicating an error condition is set, JNE addressed to the HCC results in "no jump". The status word is:





The status bits have the following meanings:

Transmitter Status;

TSP - The transmitter has been placed in transparent mode by an OPR S' = 6 instruction.

TBY - Transmitter is busy (transmission in progress).

EOR - End of Range. The range register is full, indicating that the maximum number of words specified by the program has been transferred.

CTS - Clear to Send from the data set interface is true.

DSR - Data Set Ready from the data set interface is true.

UNF - Underflow error. A new word was not supplied to the transmitter before the content of the preceding word was transmitted. This error would normally occur only while testing the HCC with the transmitter in transparent mode, in which case, UNF would set if the second half-word supplied by OUT S' = 4 was not supplied in time.

Receiver Status;

TSP - The receiver has been placed in transparent mode by OPR S' = 4, 5, or 7.

RBY - Receiver Busy (reception in progress).

EOR - End of Range. The range register is full, indicating that the maximum number of words specified by the program has been transferred.

EOM - End of Message. A REND word has been received from a remote station.

CD - Carrier Detected. The carrier detect line from the data set is true, indicating that the data set has detected the carrier from a data set at a remote station.

EXT - External input. A special external input line receiver is provided on the data set interface and this bit indicates that the signal is true. This is not a standard RS232C signal and in most applications, this bit should not set.

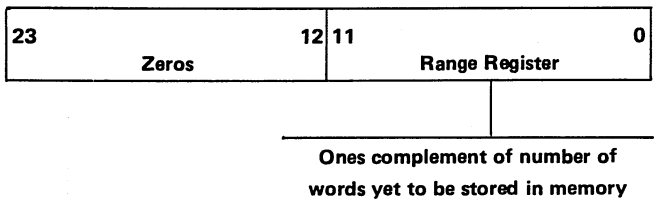
OVF - Overflow error. A received word was not stored in main memory before it was replaced by a new word received from a remote station.

RTO - Remote Timeout error. Indicates that the addressed remote station did not reply to a computer command before a timer in the HCC timed out. The timer operates only after it is set by OPR S' = 0 or 1. Since the remote stations do not reply to RAPT, STRE, and RSET commands, the timeout for them is normal.

BCH - A BCH error. A check segment error was detected by the receiver. Received words in which BCH errors were detected are indicated by ones in the memory location in which the received word would have been stored if no error was detected.

BPE - Bus Parity Error. The GENIE Bus controller detected an error on data provided by the HCC receiver.

IN S' = 3 = Interrogate range register. Transfers the contents of the HCC range register to the AU's A Register. This instruction has no other effect and may be executed at any time. The A Register content is:



JCB S' = 2 = Jump if Channel Busy. If the jump occurs, the HCC transmitter is busy transmitting a command or the receiver is busy receiving a reply (or a test word is being transmitted and received via the test plug).

JDR S' = 4 = Jump if Data Ready. This instruction is used for test purposes, only. It is used to determine when the HCC transmitter is ready to accept OUT S' = 4 instructions while in transparent mode, and it is used to determine when the receiver is ready to transfer test words via IN S' = 0.

JNE S' = 0 = Jump if No Error. If no jump occurs, one or more of the errors indicated by HCC status bits 15, 3, 2, 1, or 0 has been detected.

13.5.5 HCC Interrupt

The HCC makes a type 1 interrupt request only. Four conditions cause this interrupt to be requested:

End-of-Message. Receipt of a REND word from a remote station. The EOM status bit (see IN S' = 2) will be set.

Program Activated by ACT S' = 2.

Remote Time Out due to a lack of response from a remote station. The RTO status bit (see IN S' = 1) will be set. The absence of a remote station response to RAPT, STRE, and RSET commands is normal. Lack of response to all other commands is abnormal. The timer is started only when a command is transferred by OPR S' = 0 or 1.

Range Register Echo indicates that the word count has decremented to zero.

13.5.6 Line Turnaround

The HCC to remote stations communications channel is half-duplex, i.e., transmissions occur in both directions, but not simultaneously. This means that when two-wire communications lines are used, the line must be turned around when changing the direction of transmission. In four-wire operation with a single remote station, both the HCC and the remote station may hold Request to Send on continuously, and Clear to Send from the data sets will be on continuously, as will the data set carrier signals. On a four-wire party line to up to 29 remote stations, the HCC's Request to Send and data set carrier may be left on continuously, thereby minimizing turnaround at the computer end; but the remote stations must turn on Request to Send and, therefore, their data set carrier, only when replying to a computer command, so while line turnaround time is reduced, it is not eliminated. For two-wire lines, both the HCC and the remotes must control their data set carriers with Request to Send, and the data sets must withhold Clear to Send long enough to allow the carrier to be established on the entire channel. Two-wire lines, therefore, require the greatest line turnaround time, which may be 20 milliseconds or more.

13.5.7 Additional Features

Device Addresses and API's: The HS7024 Communications Coupler uses a single GENIE Bus device address and generates a single API (13.5.5).

Environmental Class: A. (See 3.1.)

AUXILIARY SYSTEM CABINETS

Auxiliary System Cabinets are of the same basic size, construction and appearance as the 4500 CSU cabinet. They hold electronic modules and I/O devices that can't be put in the CSU cabinet due to space limitations. They often hold shared devices such as the Large Core Store memory or a slave I/O bus used by several processors (see Fig. 4.4 in this publication).

There are two basic types of cabinet configurations; the Auxiliary Expansion (AX) cabinets and the Video Expansion (VX) cabinets. The model variations shown below are configured to provide proper space, power, and cooling ducts for the equipment listed. AX and VX cabinet options include the frame, suitable power supply(s), and two doors. Door lock kits, side skins, the a.c. power outlet strip and I/O chassis are additional options. Each cabinet contains a filtered plenum chamber and ducting.

The cabinet models listed are designed to hold certain standard equipment but other items can often be substituted. In such cases, refer to the factory for configuration rules.

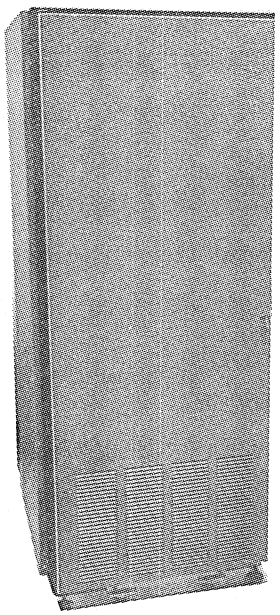


Fig. 14-1 Auxiliary Expansion Cabinet

Auxiliary Expansion Cabinets

Model	Capacity	I/O Bus Drive*
AAXC11	Up to three I/O chassis and one LCS with or without MAC.	One switch
AAXC12	Up to three I/O chassis and one LCS with or without MAC.	One extender
AAXC13	Two to six I/O chassis	Two switches (max)
AAXC14	Four to six I/O chassis	Two extenders (max)
AAXC15	Up to two LCS units with or without a Multi-Access controller for each.	

Video Expansion Cabinets

AVXC11	Up to two HPV-2 (color) video chassis	N/A
	or	
	Up to two I/O chassis	One switch
	or	
	Combinations of the two but not more than three chassis total	

Model	Capacity	I/O Bus Drive*
AVXC12	Up to three HPV-2 video chassis and one LCS with or without a Multi-Access controller.	
	or	
	Up to two I/O chassis	One Extender
	or	
	Combinations of the two but not more than three chassis total	
AVXC13	Up to three HPV-2 video chassis and up to three I/O chassis.	Two switches (max)
AVXC14	Up to three I/O chassis and up to three HPV-2 video chassis.	Two extenders (max).
AVXC15	Up to two I/O chassis on switched bus and up to two HPV-2 video chassis but not over three chassis maximum**	One switch
	and	
	Up to three I/O chassis on non-switched bus.	One extender

Associated Options

Model	Item
AIOC101	Eight-slot I/O expansion chassis
APRS101	Ac power outlet strip
ADRL101	Cabinet door lock kit
AXBE11 and AXES11	See section 4.5.6 of this publication for a discription of Bus Extenders and Extender switches.

Notes:

LCS = Large Core Store Memory
MAC = Multi-Access Controller

* The type and maximum number of Bus drivers are dictated by power system considerations within the cabinet.

** Limitation is due to power rather than space.

Input Power: Cabinet power entry provides two sequenced and two non-sequenced 115 V ac outlets. The optional ac power strip may be plugged into either type outlet. One or more of four different types of power supplies are used in the auxiliary cabinets. All of them require 104-127 V ac, 47-63 Hz single phase three wire (high, neutral and safety ground). The power system is non-sequenced but provision has been made to sequence it (from a CSU) if desired.

Environmental Classes: The Auxiliary cabinet's environmental class is determined by its contents. For the standard equipment listed in this section, class A environmental specifications apply.

Dimensions: The AX and VX cabinets are standard 76" H x 30" D x 32" W (1854mm x 812.8mm x 819.1mm).

FLOPPY DISC SUBSYSTEM

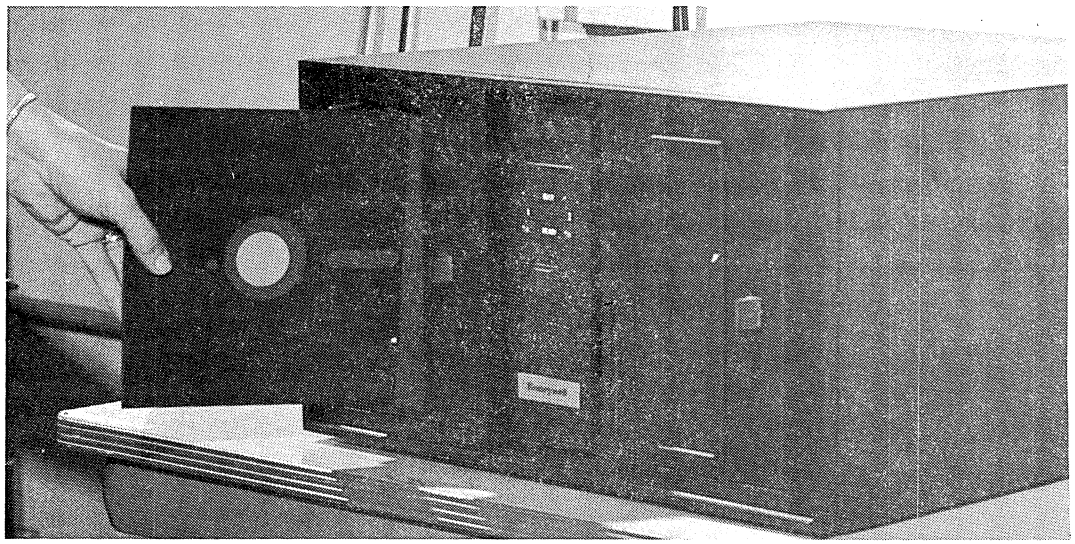


Fig. 15-1 Floppy Disc Unit

15.1 DESCRIPTION

Floppy Disc subsystems consist of an AXFD11 controller interface board and an AFDD1 Floppy Disc Unit (see Fig. 15-2). The controller board plugs into the computer's GENIE I/O Bus. It connects to a table-top Disc Drive Unit through a fixed length cable. Transfers between the GENIE Bus and controller board are at an average 10.4 k words per second. Transfers between the controller board and Floppy Disc Unit are on a byte basis. The Floppy Disc Unit accepts and stores a burst of 128 bytes (one sector) before writing on the diskette.

15.1.1 Disc Drive Units

Floppy Disc Units contain one or two disc drives. Fig. 15-1 shows a dual drive unit. Diskettes slide through the front panel openings. The disc drive records on single sided diskettes and each diskette can store/readback up to 242,944 8-bit bytes from the computer's main memory.

15.1.2 Diskettes

Diskettes are purchased with pre-recorded address headers (IBM 3740 compatible format). Track 1 of the first diskette is intended to hold a program load routine (first sector) and index information. Tracks 1 through 73 may each hold 26 sectors of data and each sector holds 128 8-bit bytes of data. Diskettes have a total capacity of 1898 data sectors or a total of 242,944 8-bit bytes.

15.2 OPTIONS

Floppy Disc Units may contain either one or two disc drives. Disc units are available which operate on either 50 or 60 Hz power. A single Floppy Disc controller board can drive either the single or dual Floppy Disc Unit.

The controller board may be placed in any available GENIE Bus slot. It contains miniature switches to select the GENIE Bus address, and interrupt/DMA service priorities. The interface controller board and disc drive unit connect with a 25 foot cable.

15.2.1 Model Numbers

Model numbers are:

AXFD11 - Floppy Disc controller interface board

AFDM11 - Diskette, single surface with write protect slot

AZFD11 - Cable, controller to drive unit, 25 foot (7.6 m) fixed length

AFDD1X - Floppy Disc Drive Unit

X = 1 - Single disc, 50 Hz
X = 2 - Dual discs, 50 Hz
X = 3 - Single disc, 60 Hz
X = 4 - Dual discs, 60 Hz

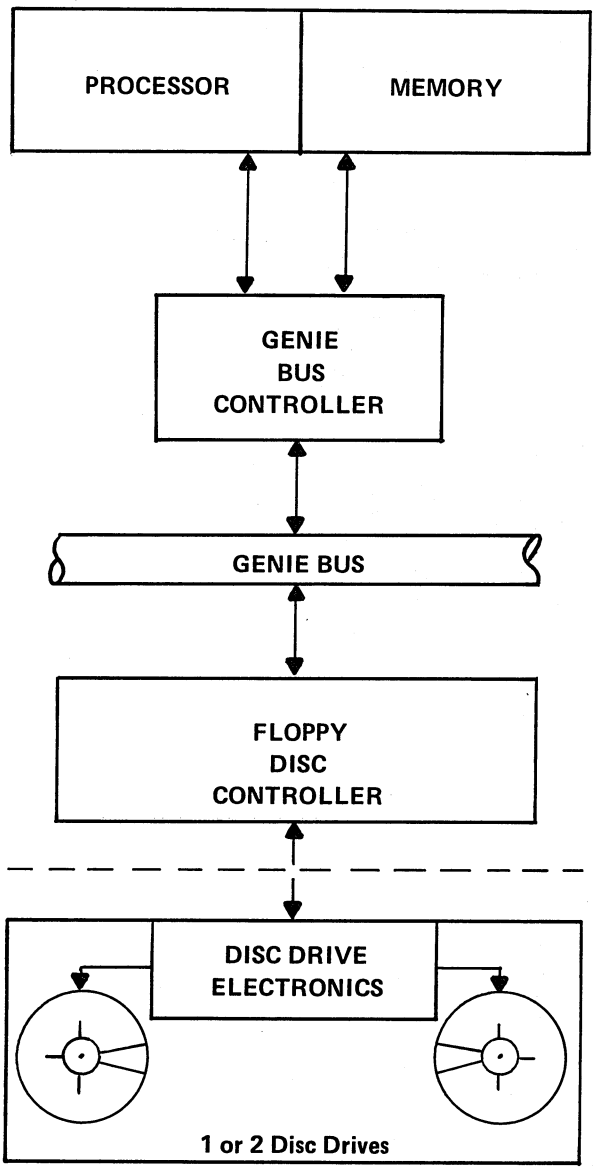


Fig. 15-2 Block Diagram - Floppy Disc Subsystem

15.3 FEATURES

15.3.1 Write Protection

An entire diskette may be write protected by uncovering a slot in the diskette's jacket. Covering the slot again permits write operations.

Track 0 is protected from write operations unless a "track 0 write-allow bit" is set in the operation code (15.4.1). Track 0 normally contains indexing information and on the first drive unit, it may also contain a program load routine.

15.3.2 Access Time

Access time includes latency time and head movement time. Latency time is the time required to find the selected sector. Obviously it is a function of rotational speed. For the Floppy Disc, average latency time is 83 msec with a maximum of 173 msec. Average head movement time is 320 msec and varies from 80 msec for a single track to 830 msec maximum.

15.3.3 Validity and Error Checking

Before writing or reading, each address header is verified by reading a header cyclic redundancy check (CRC) character. After writing each sector, a data CRC check character is automatically recorded. The data CRC character is verified from each sector on readback. Transfers between the GENIE Bus and the Floppy Disc controller board are checked for odd parity. Disc unit errors are flagged in a termination status word (see Fig. 15-3b).

15.3.4 Recoverable Error Rate

The recoverable error rate does not exceed one in 10^9 bits transferred at a 90% confidence level. Recoverable means up to ten read/write attempts may be necessary to successfully complete a transfer. Unrecoverable read error rates do not exceed one in 10^{12} bits transferred at a 90% confidence level.

15.3.5 Power Shutdown

Data on the diskette is preserved during power failures or intentional shutdown. If power is lost while writing on a diskette, the sector of data being written may be destroyed. After power is restored, the disc must have time to regain rotational speed. The program should attempt to read one sector from the disc and check for normal termination status.

15.3.6 Program Load

The first sector (128 bytes) from track 1 of disc unit 0 may be read into main memory locations $0\text{-}52_8$. The upper eight bits of loaction 52_8 (129th byte) are zeroed. Program load operation is initiated by simultaneously pressing "RESET" and "5" at the Programming and Maintenance Console (also see Operate, S' = 0 instruction under 15.4.4). If the transfer is not completed, the Floppy Disc subsystem automatically repeats the operation until it is successful. For RESET/5 console initiated program load operations, the Floppy Disc controller board must have its GENIE Bus address switches set to 4006_8.

15.4 OPERATION

Up to 255 sectors (32,640 bytes) of data may be transferred in one command operation. The minimum transfer is one sector (128 bytes).

15.4.1 Setup

Before starting a transfer, the program sets up a Request Table in main memory. A Request Table contains from one to ninety consecutive groups, of four words each (see Fig. 15-3a). Each four word group describes one transfer operation (e.g., disc address, main memory address, number of sectors to transfer and which way).

As shown in Fig. 15-3, bits 23 - 16 of control word 4 contain an operation code. The operation codes are as follows:

010 000 00 - Read data

Data is read from the specified disc address into main memory starting at the address specified in CW3.

101 W*00 00 - Write Deleted Record

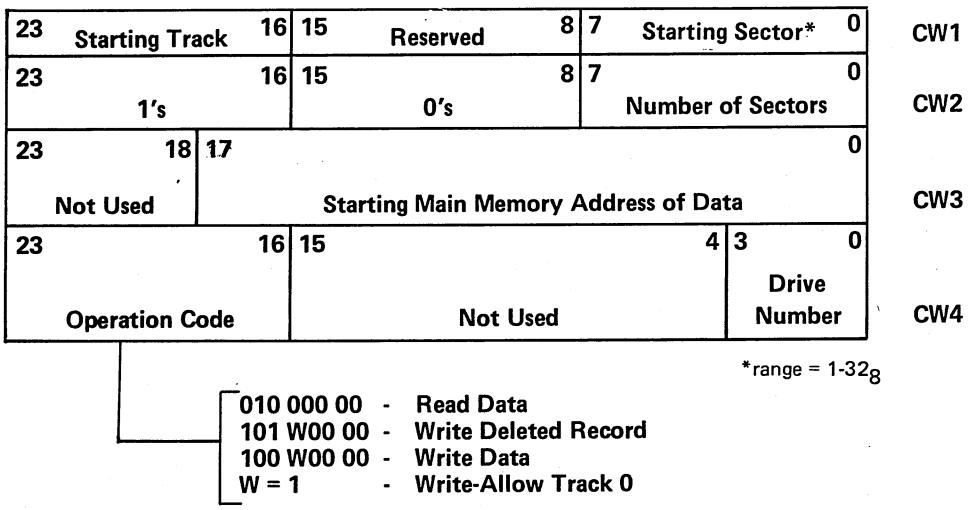
Data from main memory is written on the disc beginning at the address specified in CW1. If W=0, the beginning track address must be greater than 0. A deleted record code is also written onto each sector involved. When read back, the deleted record code is indicated in the termination status for any sector affected.

100 W*00 00 - Write Data

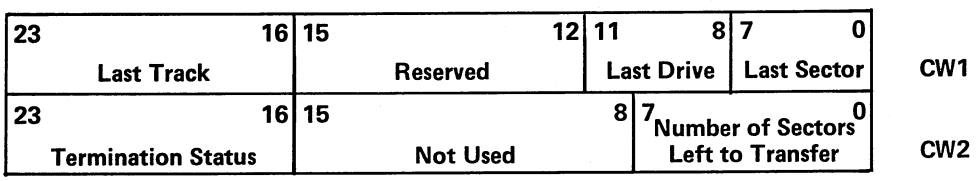
Data from main memory is written on disc beginning at the address specified in CW1. If W=0, the beginning track address must be greater than 0.

*W is the track 0 write-allow bit. When W=0, track 0 is protected from write operations.

If W=1, the write operation may begin on track 0.



a. Four Word Request before Transfer



b. CW1 and CW2 after Transfer

Fig. 15-3 Control Word Format for Data Transfers

111 000 00 - Reset

Reset returns the disc drive specified in CW4 to track 0. Controller hardware is not reset by this operation code and a normal termination status results. The request table and termination status for Reset is shown in Fig. 15-4.

15.4.2 Transfer Sequence

After the program sets up a request table, the A-register is loaded with the beginning memory address of this table. An Operate (S'=2) instruction moves A-register data to the Floppy Disc subsystem. Next, the A-register is loaded with a number from 0-131$_8$ to specify which four word group should define the transfer. An OUT instruction moves A-register data to the controller and begins the operation. After examining the selected four word request group, the controller board addresses a disc drive and begins the operation.

Transfers between the GENIE Bus and the controller board are by Direct Memory Access (DMA) at an average 10.4 k word/second rate. Data may be transferred to or from any main memory location 0 through 262,144$_8$. Transfers between the Floppy Disc Unit and the controller board are on a byte basis. Both the disc unit and the controller board can buffer (store) up to one sector of data.

As the transfer operation concludes, control words 1 and 2 of the request group are overwritten with termination information (see Fig. 15-3). This identifies the last disc address accessed, the number of sectors left to transfer (if the operation was not completed), and a termination status. Finally, the processor is signaled with an end-of-operation interrupt.

15.4.3 Termination Status Codes

Following an attempted transfer operation, the termination status bits loaded into CW2 have the basic form shown in Fig. 15-5. Table 15-1 lists the possible termination codes and explains their meaning.

15.4.4 GEN 2 Instructions

Floppy Disc subsystems are controlled and monitored by GEN 2 instructions which have the following basic format:

2 5 X S D D S' D

Where X = index field
S = type of action
S' = sub-action bits
DDD = device address on GENIE Bus

Actions caused by the S and S' bits are as follows:

Activate Interrupt (ACT), S=1, S'=0

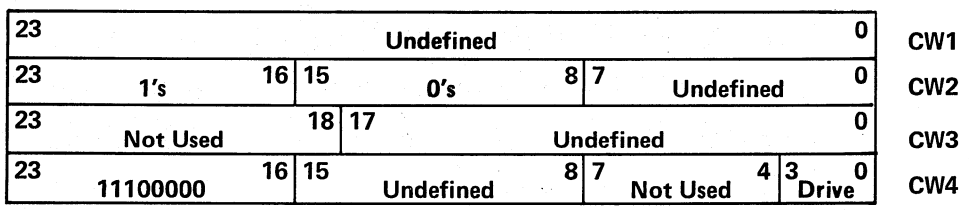
ACT sets an interrupt request (if the controller is not busy). It should be preceded by a JNR to be sure the controller is ready.

Activate Interrupt Mask (AIM), S=1, S'=6

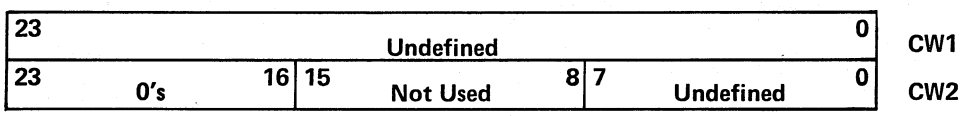
AIM blocks interrupt requests from the controller. Interrupts are not lost but are held until released by the DIM instruction.

Deactivate Interrupt Mask (DIM), S=1, S'=7

DIM permits interrupt requests from the controller. DIM is the opposite of an AIM instruction.



a. Before Operation



b. After Operation

Fig. 15-4 Reset Operation

Program Load (Operate), S=2, S'=0

This instruction causes the Floppy Disc subsystem to transfer the first sector of data from track 1, drive 0, unit 0 to main memory location $0\text{-}52_8$. The lower byte of location 52_8. (129th byte) is set to 0. If the transfer is not completed, the subsystem stays busy and keeps trying to complete the operation. The program load operation is also caused by simultaneously pressing keys RESET and 5 at the Programming and Maintenance Console, and switching to Run Mode. The bootstrap routine must be coded so as to transfer the controller's address into memory location three.

Operate (OPR), S=2, S'=2

OPR, S'=2 causes the controller to load A register bits 17-0 (address of the request table). It should be preceded by a JNR instruction to be sure the controller is not busy. An end - of - operation interrupt results from this instruction.

Abort (ABT), S=3

Conditional Abort, S'=0

This instruction causes Floppy Disc operation to stop in an orderly manner. If a transfer was in progress, it halts at the end of the current sector. The subsystem will test busy until abort action is completed. Neither termination status nor an interrupt is generated.

Unconditional Abort, S'=1

This instruction causes an immediate halt to any subsystem operation. If a transfer is in progress, data may be lost. Control and status monitoring circuits are initialized, thus neither status nor interrupt is generated.

CW2 Bits 23 - 16	Meaning
000 000 00	Normal termination - No error.
000 010 00	Deleted record was read.
100 100 00	Attempted to write on protected track 0, or hardware failure in the Floppy Disc Unit. To write on track 0, a write-allow bit must be set in the operation code.
100 100 10	CRC (check character) error on address or data.
101 100 00	Diskette is write protected (edge slot is exposed).
101 100 01	Seek error (unable to find the assigned track).
101 100 10	Illegal command to the Floppy Disc Unit - - e.g., impossible track or sector address.
101 100 11	Buffer overload (information is not flowing properly between controller and Floppy Disc Unit).
101 111 00	The selected disc drive is not ready or has not been ready at some time since last operation.
110 100 01	Overrun. The GENIE Bus did not transfer data as fast as the controller required.
111 000 00	Parity error on data from main memory.
111 000 01	GENIE Bus/Disc Controller transaction error.
111 000 10	Addressing error on GENIE Bus transaction.
111 000 11	An OR status of any of the previous three errors.
111 111 11	No transfer (original contents of CW2).

Table 15-1 Termination Status Codes

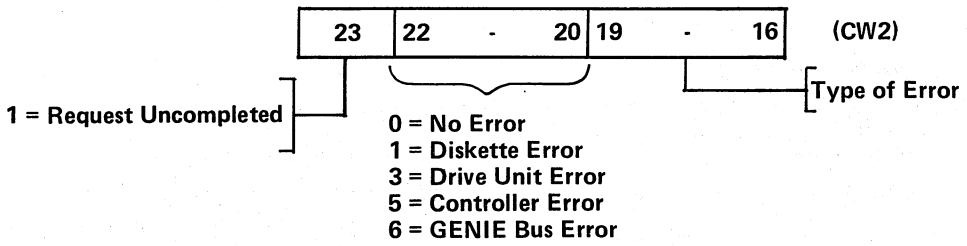


Fig. 15-5 Basic Termination Status Format

OUT, S=4, S'=0

A register bits 0-23 are sent to the controller and an operation begins. A register data at the time of the OUT is the request group number ($0\text{-}131_8$). A JNR instruction should precede the OUT to be sure the controller is ready.

IN, S=5, S'=0

If a (firmware) background test fails, IN reads the failing test number into bits 15-8 of the A-register, used by hardware test programs.

Jump If Not Ready (JNR) S=6, S'=0

JNR tests the ready/busy state of the Floppy Disc controller. The controller is busy during these operations:

While transferring or attempting to transfer data.

When loading the request table address.

While activating an interrupt.

When aborting an operation.

Jump If No Error (JNE), S=7, S'=0

JNE tests the controller's alarm line. Controller alarms result from transfers between the GENIE Bus and the Floppy Disc's controller interface board. JNE does not sense Floppy Disc Unit errors (which do appear in the termination status).

15.5 OTHER CHARACTERISTICS

15.5.1 Physical

Controller - Standard 25.4 cm (10") by 38 cm (15") MEPS/GENIE Bus printed wire assembly.

Floppy Disc Unit - Front width 48.0 cm (18.9"), Rear width 45.3 cm (17.8"), Length 55.2 cm (21.7"), Height 26.5 cm (10.3"), Weight (dual drives) 31.7 kg (70 lbs).

15.5.2 Power

Controller - Uses internal 5 V power.

Floppy Disc Unit - 110 VAC $\pm$10%, 50 or 60 Hz, approximately 3.5 A.

15.5.3 Environmental

Controller - Class A, industrial (0-50°C, 5-95% RH non-condensing).

Floppy Disc Unit - Class C, office (18-29°C, 5-95% RH non-condensing).

PORTED BULK MEMORY CONTROLLER AND BULK INTER-SYSTEM LINK

The Ported Bulk Memory Controller serves as the 4500 process computer's interface to the Moving Head Disc Subsystem (Section 6) and the Magnetic Tape Subsystem (Section 17). In addition, this Bulk Memory Controller (BMC) may serve as a Bulk Intersystem Link between two or more 4500 Central Processors (CPUs). Where two or more port interfaces are implemented on a BMC serving a Disc or Mag. Tape Subsystem, the CPUs may have access to and share the mass storage afforded by those subsystems.

16.1 FUNCTIONAL DESCRIPTION

Fig. 16-1 shows the maximum functional configuration of a Ported BMC. The BMC may support one Moving Head Disc Subcontroller with one through four Disc Units, and/or one Mag. Tape Subcontroller with one through 4 Mag. Tape Units. One of each subcontroller type may be accomodated. If the Bulk ISL function, only, is needed, no subcontrollers are required.

Should only one CPU be connected to a BMC, the isolation afforded by the GENIE Bus Port PWA is not needed, and it is not implemented. To gain shared mass storage (disc and/or mag. tape) one port PWA is needed for each CPU, and of course, one port PWA is needed for each CPU in ISL operations.

The operating sequence for all three functions, disc access, mag. tape access, and ISL operation, is similar. The program in each CPU sets up the BMC to service its subsequent requests by passing the base address of a request entry table in its own memory to the BMC (OPR S' = 1, followed by 3 OUTs, followed by OPR S' = 2). Thereafter, a CPU defines each operation by placing four control words in one of 84_{10} 4-word blocks in the table. The program initiates an operation by transferring the entry number of the four control words to the BMC (OUT), and the BMC then accepts the request.

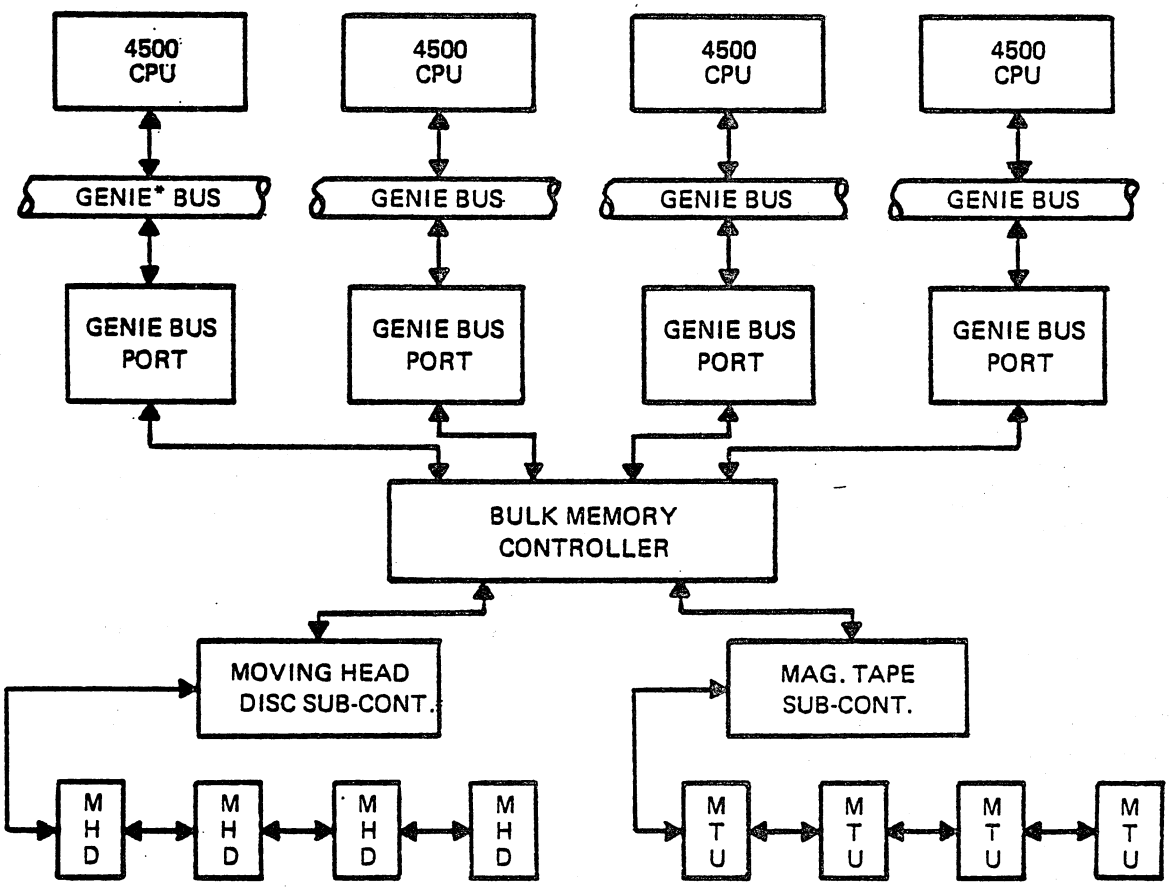


Fig. 16-1 Maximum Ported BMC and ISL Configuration

All controll word and data transactions between a CPU and the BMC are normally through the GENIE Bus direct memory access feature. The BMC goes directly to the requesting CPU's memory for the control words, examines all pending requests for operation for all CPUs, and optimizes servicing of the operations for maximum throughput. Data transferred to and from mass storage are transferred directly to or from the requesting CPU's memory and data transferred between CPUs participating in an ISL operation are through the BMC, directly to and from each other's memory. All data exchanged between CPU memories and the BMC are in the form of 24-bit data words.

For all three types of data transfer operations (disc, mag. tape, and ISL) parity is checked on the transfers through the GENIE Busses. For disc data transfers, error detection and correction are accomplished in writing on and reading from the discs. In mag. tape operations, lateral and longitudinal parity are generated and checked when writing on and reading from the tape. When a transfer is completed, the BMC stores termination status information in the same 4-word block in the entry table in the CPU from which it received the request. The BMC then requests a transfer-complete interrupt in the requesting CPU. The CPU may then read the entry number from the BMC (IN S' = 0), so that it may find the termination status in its memory and determine the outcome of the operation.

For ISL operations, the control words may specify:

- Unsynchronized data transfers in which one CPU initiates a read or write operation anywhere in another CPU's memory.
- Synchronized information transfers in which one CPU receives it, or one CPU may broadcast a message to all connected CPUs.
- Testing and manipulation of arbitration flags maintained in the BMC for operational signaling between cooperating CPUs.

This section of the 4500 General Description may be expanded to include complete detail on Bulk ISL operations, should standard software for inter-system communication be developed. Software to perform the ISL operation is presently offered on a special order basis.

For additional detail on Moving Head Disc Subsystem operations, refer to Section 6 in this General Description. For additional detail on Mag. Tape Subsystem operations refer to Section 17.

16.2 OPTIONS

16.2.1 Model Numbers

- ABMC11 Bulk Memory Controller; no port interfaces. Used with one or two mass storage subsystems (Moving Head Disc and/or Mag. Tape). May be installed in CPU or an expansion cabinet. BMC consists of two PWAs (2 slots). One PWA (1 slot) for each subcontroller. One error correction PWA (1 slot) needed for disc subsystem.
- ABMC12 Ported Bulk Memory Controller; two port interfaces. Used as Bulk ISL and/or with mass storage. Must be installed in an expansion cabinet. BMC consists of three PWAs (3 slots). One PWA (1 slot) for each subcontroller. One error correction PWA needed for disc subsystem (1 slot). GENIE Bus Port PWA (1 slot) must be installed in GENIE Bus chassis in both CPUs.
- ABMC13 Ported Bulk Memory Controller; three port interfaces. Same as ABMC12 except BMC consists of four PWAs (4 slots) and GENIE Bus Port PWA (1 slot) must be installed in GENIE Bus chassis in all four CPUs.
- ABMC14 Ported Bulk Memory Controller; four port interfaces. Same as ABMC12 except BMC consists of five PWAs (5 slots) and GENIE Bus Port PWA (1 slot) must be installed in GENIE Bus chassis in all five CPUs.

16.3 ADDITIONAL CHARACTERISTICS

16.3.1 Power

All of thes PWAs receive power and grounding from the cabinet and chassis in which they are installed. The expansion cabinet in which a ported or non-ported BMC is installed requires 115 Vac + 10% @ 47 to 63 Hz.

16.3.2 Ported BMC - CPU Interfaces

The BMC to Port PWA cables are fixed at 9 m (30') in length.

16.3.3 Environmental Class

The BMC, error correction PWA, subcontrollers, and Port Interface PWAs operate in environmental class A (see Table 3-1 in Section 3).

The Magnetic Tape Subsystem provides a very large data storage capacity at lower cost than equivalent drum or disc subsystems. The Mag. Tape Subsystem is not a substitute mass storage subsystem suitable for storage of real-time programs and data, but it is useful for storage of large amounts of data, such as historical data, for later analysis. This analysis could be done on the 4500 system or on other systems, including other manufacturers' equipment. Mag. Tape may also be used to enter programs and data into the 4500 from tapes prepared on the 4500 system or on other equipment.

The minimum Mag. Tape Subsystem consists of a Mag. Tape Controller made up of a Generic Bulk Memory Controller (BMC) and a Mag. Tape Subcontroller (MTC) installed in a GENIE I/O chassis, a Magnetic Tape Transport (MTT) in the Mag. Tape Unit cabinet, and a Mag. Tape Formatter (MTF), also housed in the MTU cabinet. The MTF interfaces with the Mag. Tape Controller, and can handle up to four tape transports, each installed in its own cabinet.

The tape transports are designed for easy reel installation and tape threading. Where a library of reels is provided very large amounts of data can be stored. A 10.5 inch tape reel containing 2400 feet of tape can store more than 10 million characters at 800 characters per inch.

17.1 FUNCTIONAL DESCRIPTION

Data is recorded on the tape in the form of 9-track characters in binary format as shown on Fig. 17-1 and Fig. 17-2. In normal operation, an odd parity bit is recorded with each character. Data is recorded on the tape in records consisting of several characters and files consisting of one or more records.

As shown on Fig. 17-3, the Mag. Tape Controller is a part of the GENIE I/O subsystem of a 4500 CPU system, which interfaces with the Mag. Tape Formatter via a 20 foot cable. The Mag. Tape Controller and the MTF are capable of handling up to four tape transports, each of which is selected for an operation by the program. The program may request a rewind operation on one unit and then initiate a read or write operation on another unit while the tape on the first unit is rewinding. The MTF and the first tape transport are installed in the first MTU cabinet. If the 2nd, 3rd, and 4th tape transports are implemented, each is installed in a separate cabinet. These must be adjacent cabinets as the tape transports are daisy-chained by 5-foot cables.

17.2 OPTIONS

The basic parts of a Mag. Tape Subsystem are:

BMC (Bulk Memory Controller)
4DP3BABMC101-104

MTC (Mag. Tape Subcontroller)
4DP3AAXMTC1

MTU (Mag. Tape Unit)
4DP3AAMTU101-206

(An MTU can be an MTF and an MTT, or it can be an MTT only.)

Mag. Tape Transports available are:*

9-Track NRZI, 75 in. per sec., 800 bpi
9-Track PE, 75 in. per sec., 1600 bpi

One Bulk Memory Controller (BMC) may have one Mag. Tape Subcontroller (MTC). The MTC accommodates one Mag. Tape Formatter (MTF), which accommodates from one to four Mag. Tape Transports (MTT). All MTTs attached to an MTF must utilize the same recording method. They must be all Non-Return-to-Zero-Inverted (NRZI), 800 bpi, or all Phase Encoded (PE), 1600 bpi. The controller is configured for a specific recording density and the transports must be compatible. Bpi refers to bit per inch per track, or characters per inch.

17.2.1 Bulk ISL Service

The same Bulk Memory Controller that serves the Mag. Tape Subsystem may also serve a Bulk Intersystem Link which interconnects up to four 4500 Central Processors. See Section 16 of this General Description.

* A 7-Track Mag. Tape Transport is available on special order. This manual does not contain any particulars on the 7-Track unit.

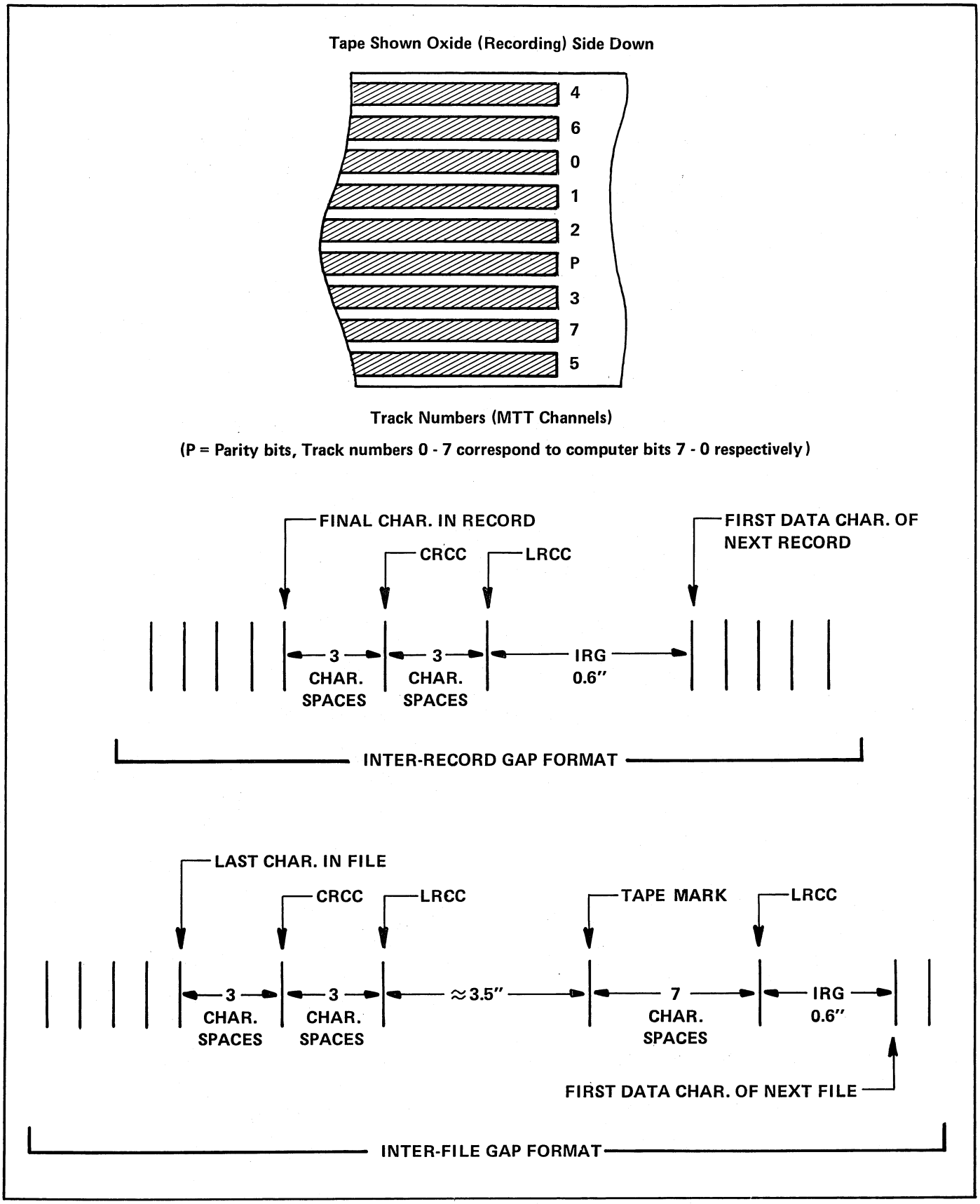


Fig. 17-1 9-Track NRZI Magnetic Tape Formats

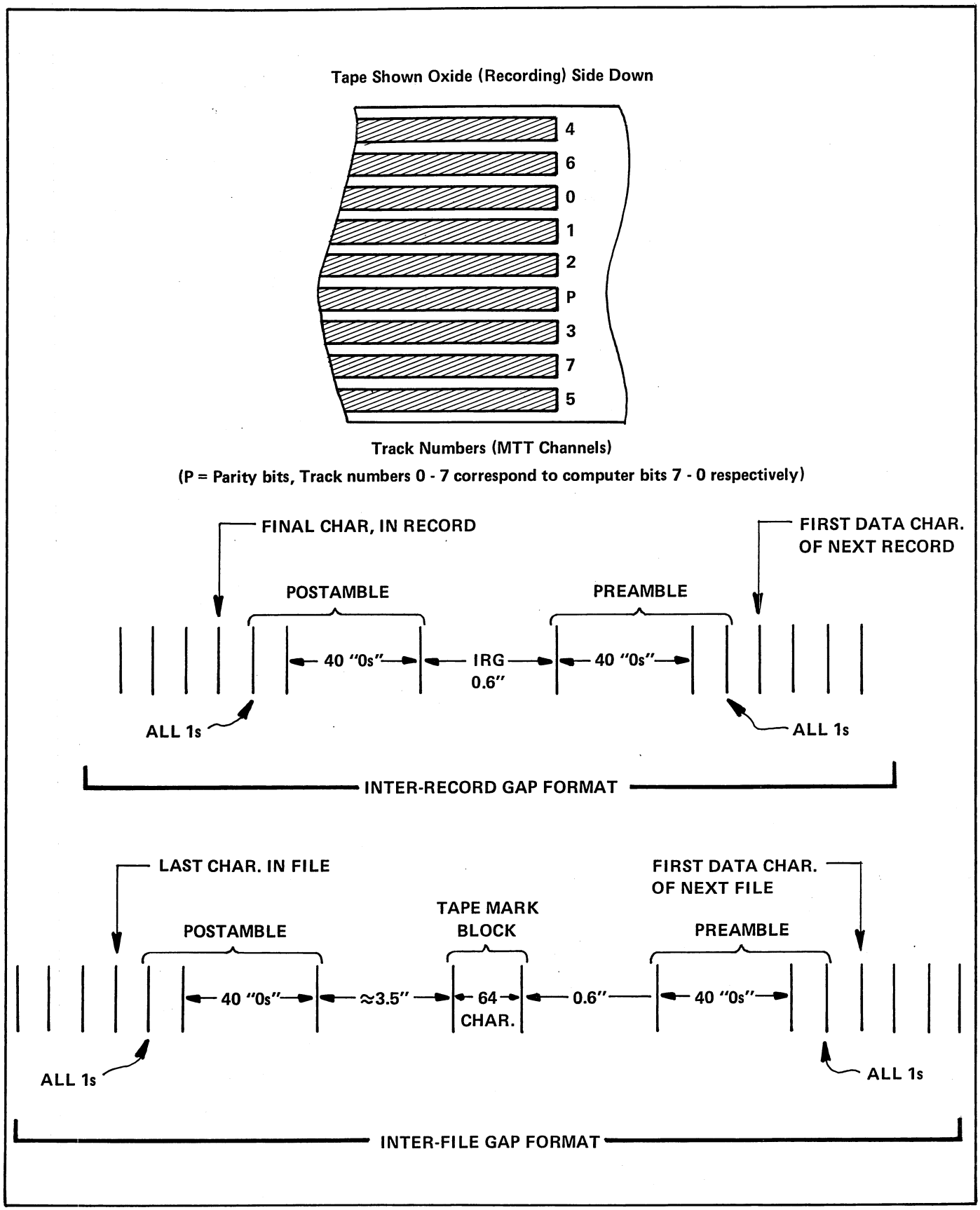


Fig. 17-2 9-Track PE Magnetic Tape Formats

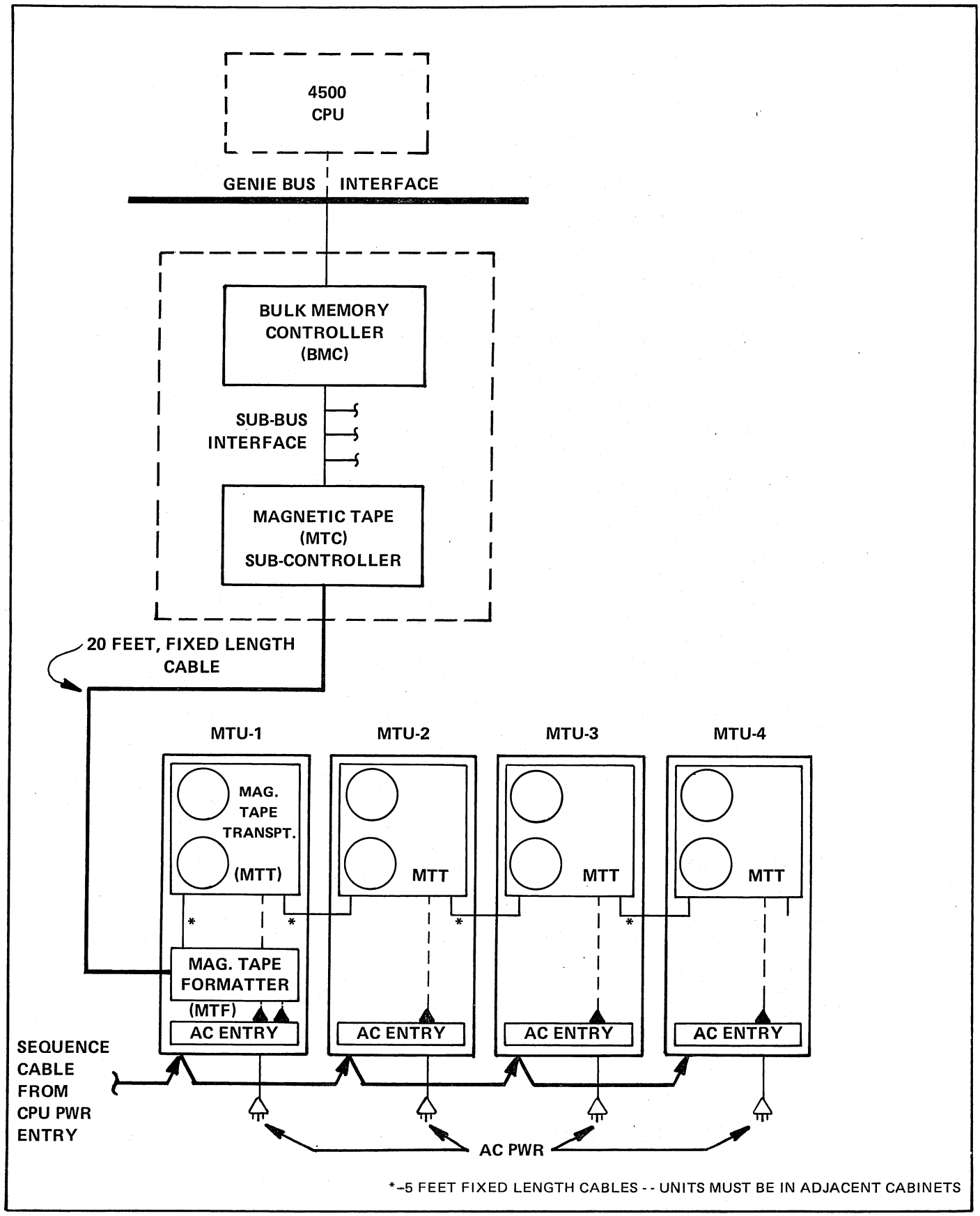


Fig. 17-3 Magnetic Tape Subsystem

17.3 OPERATING SEQUENCE

Before initiating normal operation, the BMC must receive the address of the first word of the Request Table Address Command (OPR, S' = 1), followed by three OUTs where the A-register specifies the location of the first word of the Request Table. The BMC is then placed in normal mode (OPR, S' = 2) before initiating magnetic tape operations.

Four control words dictate the parameters of each Mag. Tape Subsystem operation (see 17.4). Prior to initiating an operation, the CPU sets up the four-word entry in main memory with the M.T.S. Subcontroller (MTC), unit, read threshold, density, parity, number of words to transfer, starting memory address, initial (uninitiated) status, and operation code. The CPU performs an OUT command to the BMC with the entry number right-justified in the A Register.

The BMC receives the Request Number via the OUT command. The four control words are read from the Request Table by the BMC, using a four-word DMA read operation.

When the request is selected for transfer, the BMC re-reads the four control words from the table, marks the request entry status byte as "initiated", sets the data transfer, and transfers data between the magnetic tape and the CPU memory, using DMA and a magnetic tape equivalent buffer within the BMC.

After the request is completed, the BMC stores the termination information in the status byte of the second word of the Request Table entry. The first two control words may be modified by the BMC as the transfer proceeds. The BMC signals the CPU of the request completion by requesting an interrupt. The interrupt is acknowledged by performing an IN to read the terminated request number. This number is read in the same form that it is sent when the operation is initiated with the OUT.

17.4 CONTROL WORDS

The interaction of the controller and the Central Processor is through a Request Table located in the CPU memory. The address of the start of the request table is sent to the controller using an OPR.

Requests are stored in the Request Table as four-word entries of the form shown in Fig. 17-4. The CPU sets up an entry and then passes the entry number to the controller with an OUT command. The controller processes the request and places the termination status in the second word of the entry. The controller then signals request completion to the CPU by requesting an inhibitable interrupt. The CPU reads the entry number from the controller with an IN command. Fig. 17-4 and Fig. 17-5 detail the request and reply formats of control block words.

17.5 DATA FORMATS

The formats of the data, inter-record, inter-file and parity information written on the tape by the Mag. Tape Formatter are illustrated on Fig. 17-1 and Fig. 17-2. The relationship of the data on the tape and the data exchanged between the controller and the CPU memory is depicted on Fig. 17-6. Note that the formatter generates all non-data information written on the tape, such as tape marks, LRCC characters, CRCC characters, the preamble and postamble characters, and the inter-record and inter-file gaps, and it checks the parity bits and parity characters read from the tape, leaving only 8-bit characters to be exchanged in 24-bit words between the controller and memory. Also note that the character transferred in each 24-bit memory word is the most significant character (C0), so each block of three characters within a record on the tape represents one 24-bit memory word, running in the following sequence: C0, C1, and C2.

17.6 INSTRUCTIONS

17.6.1 GEN 2 Instructions

The following GEN 2 instructions, when addressed to the Mag. Tape Controller, affect the Mag. Tape Subsystem as described.

ABT - Abort Command initiates termination of a current operation to release the subsystem for some alternate operation. Coding of the S' bit (bit 3) of the instruction word dictates the type of termination to take place:

S' = 0 - Conditional Abort. This instruction initiates an orderly termination of the current operation, as soon as any data transfer is completed. If data movement is already in progress, the operation terminates at the end of the current character. The controller goes ready and its API is generated at the time the controller action ceases. The integrity of all monitoring functions is preserved. Operations received by the controller for which no data movement has started are cleared from the controller's internal request queue. No changes are made to the CPU Request Table.

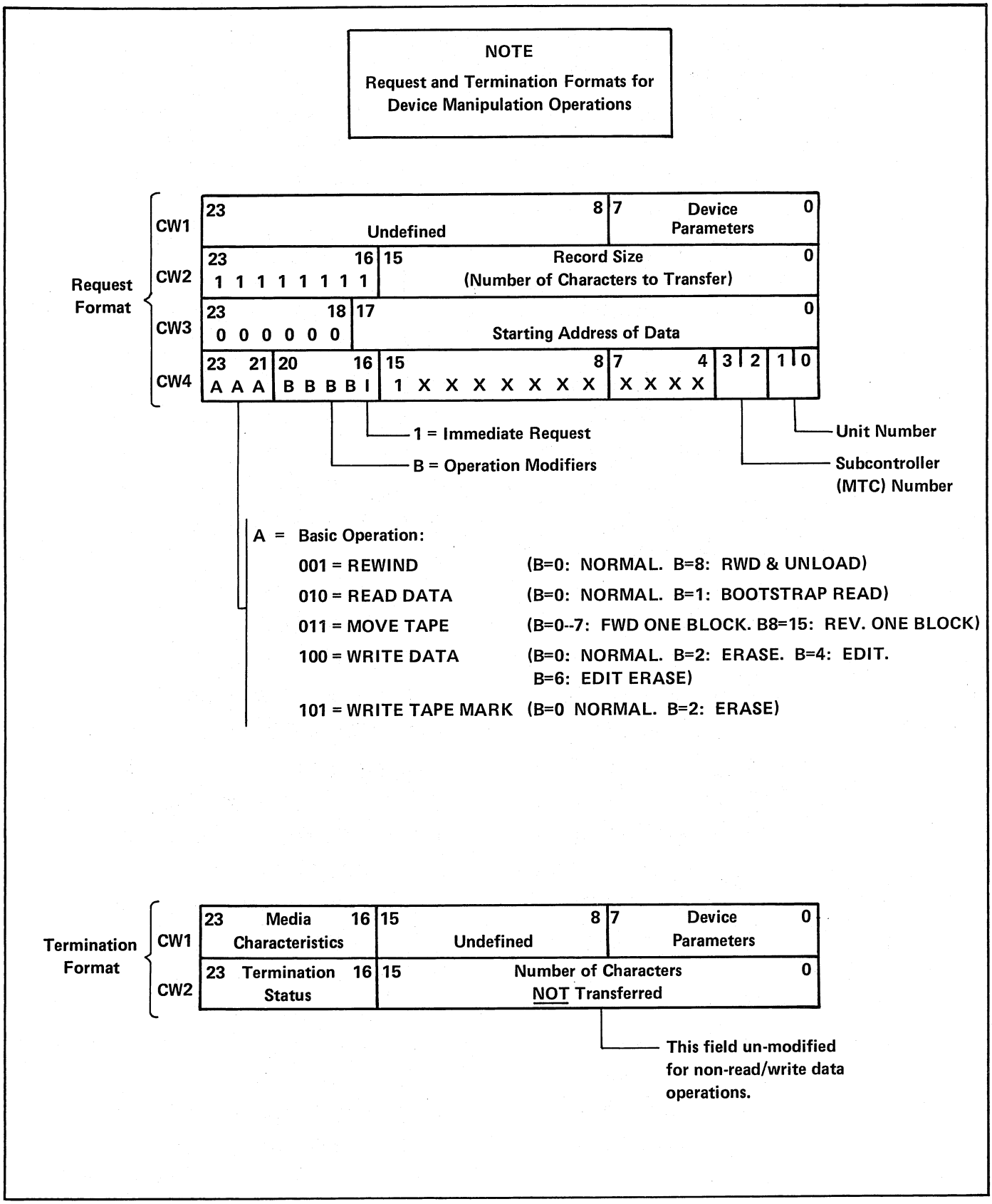


Fig. 17-4 Data Transfer and Device Control Word Formats

NOTE

Request and Termination Formats for Control/Test/Status Operations

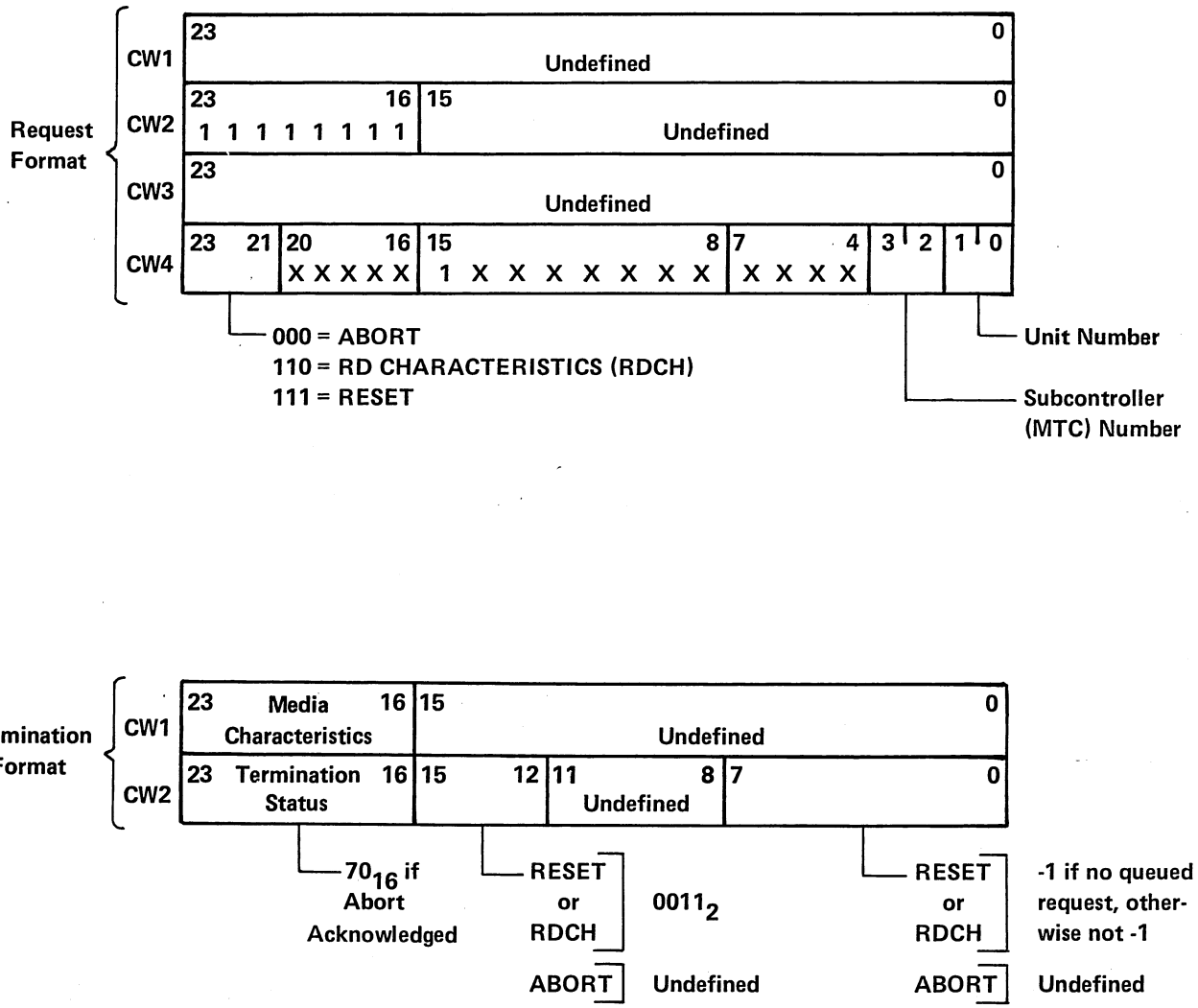


Fig. 17-5 Control/Test Control Word Formats

MEMORY BIT POSITION	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTU POSITION	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
MTU BYTE POSITION	C_0								C_1								C_2							
BINARY WEIGHT	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Fig. 17-6 Memory/Tape Data Format

S' = 1 - Unconditional Abort. This instruction causes a complete unconditional initialization of the Mag. Tape Controller immediately, or at the completion of any memory cycle in progress. All operating and monitoring functions are cleared, the controller goes ready, and its API is generated. Manually initializing from the Programming and Maintenance console has the same effect. Data to be written on the tape may be lost, and any information written on the tape immediately prior to the Unconditional Abort will not be delineated by inter-record gap information. It is the responsibility of the user to regain memory unit synchronization and recover from any data destruction that may occur.

ACT - Activate Interrupt Command generates a processor interrupt. The S' field (bit 1) defines the operation of the command as follows:

S' = 0 Sets the inhibitable interrupts as if the MTS has completed operation.

S' = 6 AIM - Activates the interrupt mask, blocking interrupt request.

S' = 7 DIM - Deactivates the interrupt mask, permitting interrupt requests.

IN. The S' bit (bit 5) defines the operation of the command as follows:

S' = 0 - Receive Data from Controller. Bits 0 - 7 of the A Register are set by the controller and the interrupt request, if present, is reset. The meaning of the data depends on the mode set by a previous OPR command.

If the controller has not set its CPU interrupt, the data received in bits 0 - 7 is meaningless. Bit 23 of the data received is set if no interrupt request is present, indicating that the data is invalid. Bits 8 - 22 are reserved for status information and are set to zero at this time.

S' = 1 - Copy Data from Controller. Operation and data transfer is identical to IN S' = 0, except that the interrupt request is not reset and the data output latch of the controller is not cleared. The instruction is useful in polling the controller without interrupts for test purposes. The following code should be used to take data from the controller without interrupts:

```
IN /10,3    Read interrupt-present state
TOD 23      Interrupt-present?
BTS *-2     No. Try again
IN 0, 3     Yes. Read interrupt data and clear interrupts
  .
  .
  .
```

JNE - Jump No Error Command tests the Alarm Status, which indicates an error in the GENIE Bus interface to the controller. JNE has no effect on the operation of the Mag. Tape Subsystem and may be executed at any time.

JDR - Jump Data Ready Command tests the status of the MTS ready line when the S' bit (bit 6) = 4. It will appear Not Ready if the input queue of the BMC is full. Do not issue an OUT command if a controller is Not Ready.

JNR - Jump Not Ready Command tests the status of the BMC ready line when the S' bit (bit 6) = 0. It will appear Not Ready if the input queue of the BMC is full. Do not issue an OUT command if a controller is not Ready.

OUT - Send Data to Controller initiates an operating sequence as described under 17.3. The operation of the controller depends on the mode set by a previous OPR command. If the OPR mode is S' = 1, the OUT command sends the Request Table Address, if the OPR mode is S' = 2, the OUT command sends the entry number, and if the OPR mode is S' = 3, the OUT command sends the data that is returned via interrupt IN. If more than 64 OUT commands are sent to the controller in rapid succession, the controller input queue becomes full.

OPR controls the operation of the controller depending upon the mode set by the S bit (bit 2).

S' = 0 - Program Load. The MTS goes to a Not ready status, then initiates the operation sequence.

The controller reads up to 65,535 characters of data from subcontroller 0, starting at location 0 in memory. If the transfer completed successfully, the MTS returns to a Ready status, otherwise it backspaces and retries three times, then remains in a Not Ready status.

S' = 1 - Load Request Table Address. The controller goes to the Load Request Table Address mode. The Request Table Address is then loaded using three OUTs. The address bits 0 - 7 are sent with the first OUT, bits 8 - 15 with the second OUT, and bits 16 - 17 with the third OUT.

S' = 2 - Set Normal Mode. The controller is ready to receive requests via the OUT mode.

S' = 3 - Set Loopback Mode. This mode is used for testing the controller/CPU interface. The data entered into the A Register by an OUT command is returned by an IN command. (Used for test purposes only.)

S' = 4 - Set Idle Mode. The controller initializes itself and will not respond to other commands until another OPR is issued. Initialization clears all requests but does not change the Request Table Address.

17.6.2 Control Word Operation Codes

The most significant three bits of control word 4 (bits 23 - 21) specify the operation to take place, for the Magnetic Tape Subsystem. The operation codes and the operations they initiate are as follows:

Cancel (Abort) Request (0_8). The controller immediately terminates the operation with an Abort Acknowledge status.

Rewind (1_8). The controller immediately initiates a rewind operation (bit 20 of control word 4 = 0) or a rewind-and-unload operation (bit 20 of control word 4 = 1). The unit is not ready until after the rewind is completed.

Read Data Forward (2_8). The next block of data is read from the tape using the specified operating mode (CW1 - CW3). The maximum number of characters read is "The Number of Characters to Transfer" (bit 17 of control word 4 = 0) or 65,535 (bit 17 of control word 4 = 1, bootstrap mode).

The termination status indicates whether the record read is shorter than, equal to, or longer than the buffer size specified in the request. If the record is longer, the extra characters are discarded by the BMC's mag. tape drive firmware. If the record is shorter, the termination status specifies the amount by which the record is shorter than the request.

The status indicates whether the record read is the special "Tape Mark".

Move Tape One Record (3_8). The software uses the number of units field and bit 18 of control word 4 to count down the number of records or tape marks to move past. This field is not altered by the firmware on Move commands.

The tape is moved forward (bit 20 of control word 4 = 0) or backward (bit 20 of control word 4 = 1) one record. The termination status indicates whether the record read is a data record or the special "Tape Mark" record. The specified operating mode (CW1 - CW3) applies to this request. Edit (bit 19 of control word 4 = 1) modifies the timing of the Move operation.

No data is sent to the BMC on this command.

Write Data (4_8). The specified "Number of Characters to Transfer" are written to the tape using the specified operating mode (CW1 - CW3). Edit (bit 19 of control word 4 = 1) modifies the timing of the Write Data operation to allow a previously written record, of the same length, to be overwritten without erasing part of the next record on the tape. Clear (bit 18 of control word 4 = 1) inhibits actual writing on the tape, so that an erased area appears on the tape where the data would have been written.

The following is a recommended sequence for the use of the Edit feature:

1. Read (forward) the record to be edited.
2. Move backward one record with the Edit bit set.
3. Write the new (edited) record with the Edit bit set.

Use of this feature assumes that enough space has been left between records, so that longer records will not run into records which follow.

Write Tape Mark (5_8). A special "Tape Mark" is written on the tape using the specified operating mode. Clear (bit 18 of control word 4 = 1) inhibits actual writing on the tape, so that a fixed length erased area appears on the tape where the Tape Mark block would have been written.

Read Characteristics (6_8). Status is immediately returned in CW1 and CW2. If no rewind operation is underway at the time the Read Characteristics command is issued, the status of the last request processed is returned.

Reset and Read Characteristics (7_8). Resets the sub-controller (MTC) and formatter (MTF) and immediately returns status in CW1 and CW2.

If no rewind operation is underway at the time the Reset and Read Characteristics command is issued, the status of the last request processed is returned.

17.7 DATA PROTECTION

In order to write on a tape, the tape supply reel must have a Write Enable Ring installed. If the tape reel does not have a Write Ring mounted on the tape unit, any write or erase operation is inhibited.

17.8 TERMINATION STATUS

The Termination Format consisting of CW1 and CW2 (see Table 17-1 and 17-2) contains information pertaining to requests which have either been completed or terminated. CW1 holds Media Characteristics in bits 23 - 16 and Device Parameters in bits 7 - 0 (see Fig. 17-4 and Fig. 17-5). The Termination Status Byte, bits 23 - 16 of CW2 holds alarm and error termination status.

The BMC recovers data errors and hardware failures when possible. When an error is recovered, the BMC reports the error code to the CPU in the request termination block with the non-recoverable status reset. When a data error occurs, the controller retries the operation three times to try to correct the error. Unrecoverable or fatal data errors and fatal error conditions in the GENIE Bus, subcontroller, or unit, cause the controller to terminate the operation and set a fatal error code in the termination status.

The error status reported at the completion of a request is normally the first error encountered, whether it is recoverable or not; however, if a non-recoverable error occurs, the request is terminated showing the non-recoverable error status, regardless of any previously recorded errors.

Media Characteristics: CW1, Bits 23 - 16

Bit 23	0 (zero)	
22	EOT Marker encountered	=1
21	BOT Marker encountered	=1
20	Tape Mark Record read	=1
19	Reel Write-protected	=1
18	0 (zero)	
17	Low-Density	=1
Bit 16	9 Tracks device	=0

Device Parameters: CW1, Bits 7 - 0

Bits 7, 6, 5	000 (zeroes)
4, 3	Read Threshold 0 = normal, 1 = low
2	Parity Select (7 Track), 0 = odd, 1 = even
1	Density (reserved, must be zero)
Bit 0	Number of tracks 0 - 9, 1 = 7 tracks

Table 17-1 Termination CW1 Bit Definition

23	22	21	20	19	18	17	16
F	T	T	T	N	N	N	N

CW2
TERMINATION STATUS BYTE

F = 1 Fatal - Error was not recovered by BMC
TTT = 000 - 111 - Error type code
NNNN = 0000 - 1111 - Error sub-type code

Meaning of various errors decoded from bits 16 through 23 of CW2:

Normal Termination - No Errors

F	T	T	T	N	N	N	N		
0	0	0	0	0	0	0	0	No errors - request complete	(1)
0	0	0	0	0	1	0	0	No errors - file mark read	(1)
0	0	0	0	1	0	0	0	No errors - short record read	(1)

Data Errors

F	T	T	T	N	N	N	N		
1	0	0	1	0	0	0	0	Write protected - fatal	(2)
0	0	0	1	0	0	0	1	Corrected data error - without retry	(1)
0	0	0	1	0	0	1	0	Corrected data error - with retry	(1)
1	0	0	1	0	0	1	0	Fatal data error (after retry)	(1)
0	0	0	1	1	0	0	1	Corrected data error without retry + short record	(1)
0	0	0	1	1	0	1	0	Corrected data error with retry + short record	(1)
1	0	0	1	1	0	1	0	Fatal data error (after retry) + short record	(1)

Record Structure Errors

F	T	T	T	N	N	N	N		
0	0	1	0	0	1	0	1	Apparent lack of data, recovered	(1)
1	0	1	0	0	1	0	1	No data, fatal (blank tape)	(3)
1	0	1	0	0	1	1	0	Record too long, fatal	(1)

Device Errors

F	T	T	T	N	N	N	N		
1	0	1	1	0	0	0	0	Device or media write protected - fatal	(2)
1	0	1	1	1	0	0	0	Device non-response, fatal	(2)
1	0	1	1	1	1	0	0	Device off-line, not ready, fatal	(2)

Device Adapter Errors

F	T	T	T	N	N	N	N		
1	1	0	0	0	0	1	1	Execution failed to complete, fatal	(4)
1	1	0	0	0	1	0	0	Parity error in error checking code, fatal	(1)
1	1	0	0	1	0	0	0	Error on device select check, fatal	(2)
1	1	0	0	1	0	0	1	Device adapter non-response, fatal	(2)
1	1	0	0	1	0	1	0	Device non-existent, fatal	(2)

Controller Errors

F	T	T	T	N	N	N	N		
1	1	0	1	0	0	0	1	Data transfer overrun, fatal	(1)
1	1	0	1	1	0	0	0	Controller non-response, fatal	(4)

GENIE Bus Errors

F	T	T	T	N	N	N	N		
1	1	1	0	0	0	0	0	Parity error on bus transfer, fatal	(4)
1	1	1	0	0	0	0	1	Bus check alarm, fatal	(4)
1	1	1	0	0	0	1	0	AOK latch in bus interface reset, fatal	(4)
1	1	1	0	0	0	1	1	Parity error, bus check alarm or AOK reset, fatal	(4)

Request Related Status

F	T	T	T	N	N	N	N		
0	1	1	1	0	0	0	0	No error, abort acknowledged	(4)
1	1	1	1	1	1	1	0	Request currently being serviced, transfer in progress	
1	1	1	1	1	1	1	1	Request not yet committed to transfer	

NOTES:

(1) Tape movement occurred, tape is positioned in the IRG following the last record, whether error occurred or not.

(2) No tape movement.

(3) Tape has moved approximately 25 feet without encountering data.

(4) Tape movement may have occurred, position unknown.

Table 17-2 Termination CW2 Bit Definition

17.9 CONTROLS AND INDICATORS

The basic operating controls and indicators of the tape unit are located on the front of the unit, accessible through an opening in the cover door (see Fig. 17-7). It is important to note that several of these controls operate in conjunction with the interface command lines. That is, the function of a front panel control or indicator may be affected by the status of a command line on the interface between the tape unit and the computer.

Following are descriptions of the front panel controls and indicators and of a Forward/Reverse switch which is located on the control board.

RWD — A pushbutton used to initiate a tape rewind operation that operates only when the tape unit is off-line. The tape rewinds past the BOT tab, reverses and advances to the BOT tab and stops. If the tape is at the BOT tab when the RWD button is pressed, the tape unloads (rewinds slowly off of the take-up reel).

RESET — A backlighted pushbutton that functions to stop tape motion if the tape unit is in the forward, reverse, or rewind mode, and to place the unit off-line, if it is on-line. The indicator light is on when the tape unit is selected by the computer (the proper ISELECT line is asserted).

FILE PROTECT — An indicator that lights when a write protected file reel is installed on the tape unit. The light is meaningless unless the tape is under tension in the vacuum columns.

HI-DEN — An alternate action indicator switch that selects packing density. When the switch is lighted the higher density is selected. This switch is not operational in the single density versions of the tape unit. The switch is functional in the dual density NRZI tape units or the dual density NRZI/PE tape units which are dual speed tape units, and operates in parallel with the IDDS command input line from the controller.

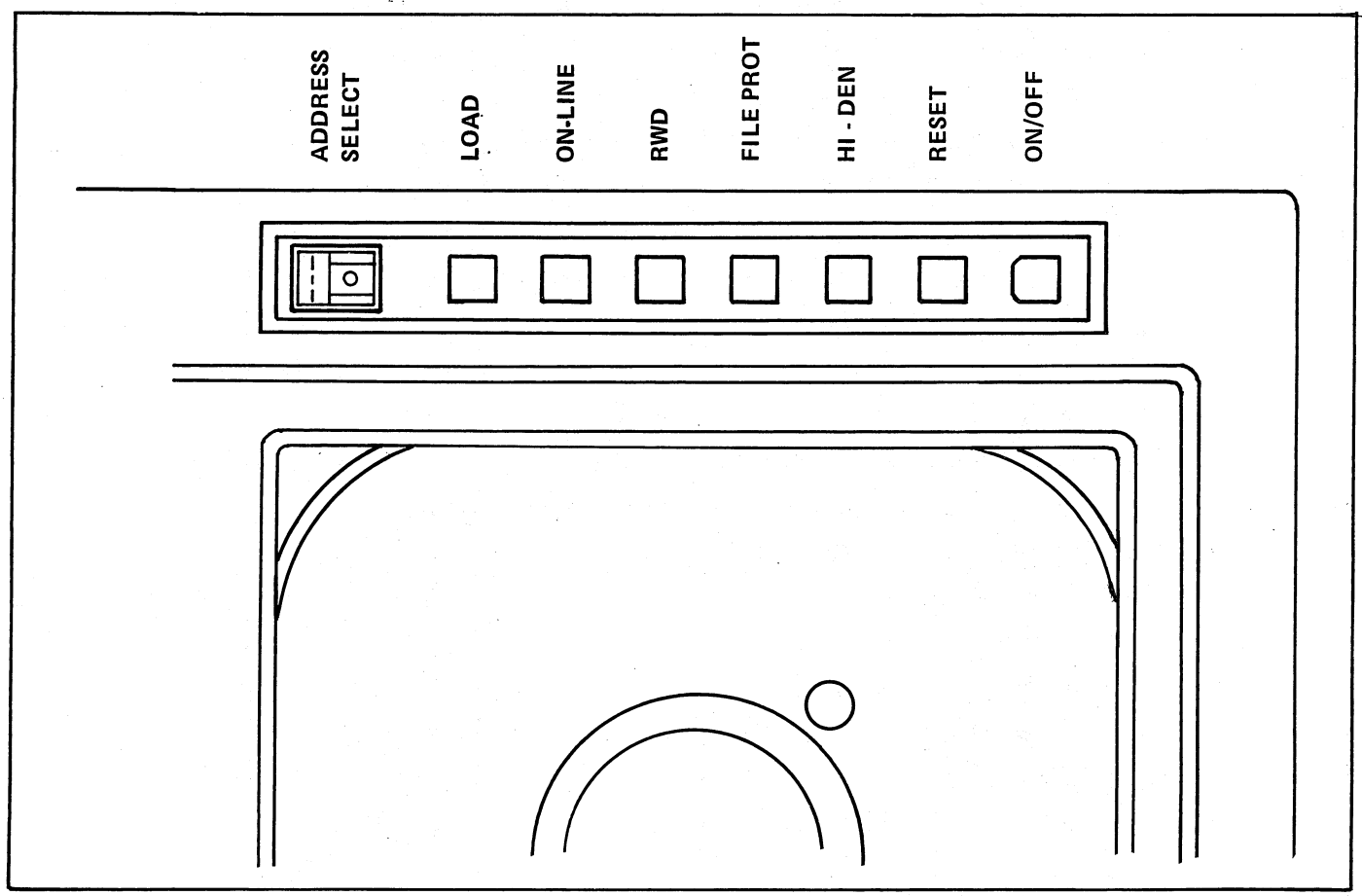


Fig. 17-7 Tape Unit Front Panel Controls and Indicators

FORWARD/ REVERSE — A three position toggle switch mounted on the tape control board, which is accessible when the tape deck is swung out. In the off-line mode, this switch can be used to move the tape in the forward and reverse directions; in the on-line mode, it has no function. This switch moves the tape only between the BOT and EOT tabs. Switch positions are: up = forward, down = reverse, center = off.

ON/OFF — A pivot switch that controls power to the tape unit; the ON side turns the power on, the OFF side turns the power off. The switch is lighted in the ON position by the +5 Volt regulator.

LOAD — A backlighted pushbutton that is used during the loading of tape. After the tape is threaded, press the LOAD pushbutton to apply tension to the tape and advance the tape to the BOT tab. The pushbutton lights to indicate that the tape is properly tensioned and has been advanced to the BOT tab. The light goes out when the BOT tab moves off the sensor.

ADDRESS SELECT — A rotary thumbswitch whose first four positions, 0, 1, 2, and 3, are used to select the active address for the tape unit. This switch operates in conjunction with the ISELECT 0 - 3 command input lines from the controller. Switch position should be changed only while the tape unit is off-line.

ON LINE — A lighted pushbutton that is used to place the tape unit under remote control (on-line). This switch operates in parallel with the RESET pushbutton and the IREU interface command line to place the tape unit under control of pushbuttons on the tape unit (off-line). Either the RESET or the IREU can place the unit off-line and extinguish the pushbutton, but cannot place the unit on-line. When the tape unit is on-line, the ON LINE pushbutton is lighted.

NOTE

The tape unit can be on-line with the pushbutton lighted, but it is not under remote control until selected by the computer. When the tape unit is selected, the RESET pushbutton indicator is also lighted.

17.10 MAG TAPE TRANSPORT AND FORMATTER CHARACTERISTICS

17.10.1 Mag. Tape Transport

Primary Power. 117 Vac ±10%, 800 W max., 48 - 62 Hz, single phase.

Physical Characteristics. One MTT is mounted in a standard 76" (1930 mm) H x 30" (760 mm) D x 32" (810 mm) W cabinet, which includes a power entry panel for customer's power connections. The first MTU cabinet also includes the Mag. Tape Formatter. Standard MTTs use a vacuum column type tape handler and accept computer grade 0.5 inch (127 mm) wide, 1.5 mil thick tape on reels up to 10.5 inches (267 mm) in diameter. The transport weighs approximately 120 lbs. (54.6 kg) and is 24" (610 mm) H x 19" (480 mm) W x 15.4" (390 mm) D. Multiple MTU cabinets must be complexed because the MTTs are daisy-chained with 5 foot (1.5 m) cables.

17.10.2 Mag. Tape Formatter

Primary Power. 117 Vac ±10%, 100 W max., 48 - 62 Hz, single phase.

Physical Characteristics. One MTF is mounted in the first MTU standard cabinet with the first MTT. The formatter weighs approximately 25 lbs. (11.4 kg) and is 3.5" (89 mm) H x 19" (480 mm) W x 20" (508 mm) D.

17.10.3 Environmental Class

The MTT and MTF operate in environmental class C.

The MTC and BMC operate in environmental class A.

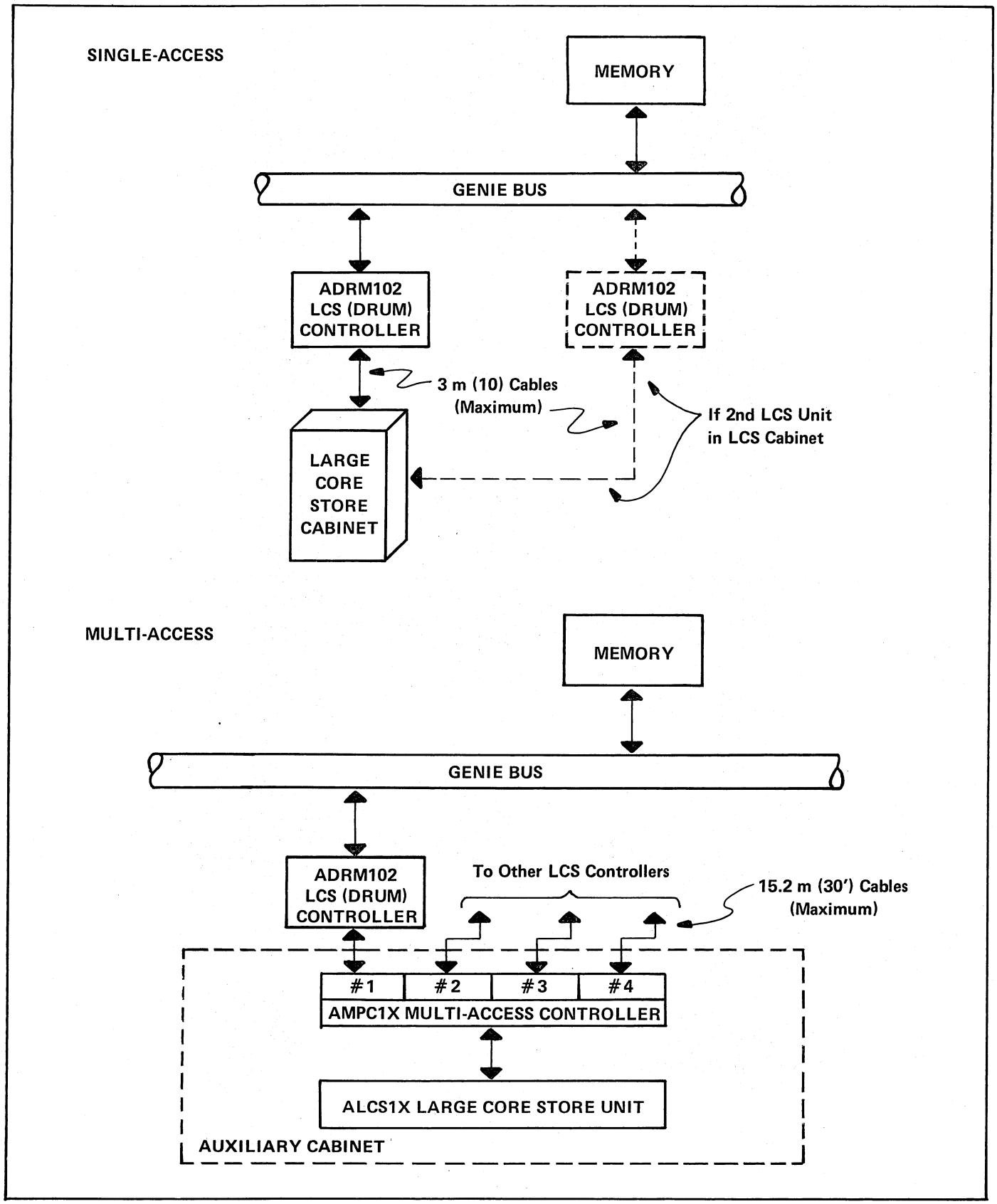


Fig. 18-1 Large Core Store Subsystems

Large Core Store is a reliable, very fast access mass storage medium for real-time programs and data that are transferred to and from main memory as needed by the running program. Large Core Store (LCS) is a large core memory implemented in an LCS unit installed in an auxiliary cabinet. The LCS unit serves as an alternate to drum memory for 4500 process computer systems, and therefore appears to the computer hardware and software as if it were a drum memory, but one that is apparently rotating about 348 times as fast as the model ADRM drum. Average access time, therefore, is 25 microseconds, compared with an average latency time of 8.7 milliseconds for the drum. Information stored in an LCS unit is retained in the unit after transfer to the computer's main memory and may be altered when re-written under control of the program.

The only significant functional difference between Large Core Store and the model ADRM Drum Memory Subsystem is access time. The same software will run on either subsystem with no modification or with only very minor modification. Software provided with General Software Release 160 bypasses the Latency Optimization feature when serving an LCS Subsystem, as it is not needed. A Multi-Access option shares the LCS with up to four 4500 computers.

18.1 FUNCTIONAL DESCRIPTION

Data are recorded in the LCS unit in tracks of 40 sectors, with 64 24-bit data words in each sector - a total of 2560 data words per track. Each 24-bit data word is the image of the corresponding word in main memory at the time the word was written in the LCS unit. Each sector also includes a preamble, a header, a polynomial check segment, and a postamble, as shown at the top of Fig. 18-2. These are all recorded each time a sector is written. The polynomial check segment contains a unique check pattern which is representative of the information in the sector. Thus, if any word in the sector is to be re-written, the entire sector must be re-written. As a sector is read, the check segment pattern is checked against a pattern regenerated while reading the information in the sector. The minimum transfer length, therefore, is one 64-word sector and all transfers must be integral multiples of sectors, up to a maximum of 255 sectors (16,320 words).

The LCS unit is available in four storage capacities in increments of 327,680 words. The largest available LCS can store up to 1,310,720 words (see 18.2 Options). Each LCS unit has an integral dc power supply and switch to turn it on or off.

The LCS cabinet's interface with the Central Processor is through an LCS controller on the GENIE Bus, which is controlled by GEN 2 instructions issued by the program (18.4.2) and exchanges data with main memory through the GENIE Bus Direct Memory Access port (4.5.4). The LCS Subsystem is capable of accessing any location in dedicated memory within 262,144 words (see the footnote on Fig. 18-2).

18.2 OPTIONS

18.2.1 LCS Controller Options

The LCS controller on the GENIE Bus has device address and interrupt priority selection controls on the printed wire boards that permit selection of any of the available 256 GENIE Bus device addresses, and any of 15 API and direct to memory request priorities that are subsidiary to the priority (1 of 16) of the Slave Bus on which the controller is installed. If the controller is on a Master Bus section, one of the 16 Master Bus priorities is selected. (See 4.5 and Fig. 4-4). Device address 404_8 must be selected for the LCS controller serving an LCS unit to be used as a bulk program load device.

18.2.2 LCS Options

Fig. 18-1 shows possible LCS Subsystem configurations. One or two LCS units may be installed in an auxiliary cabinet. One or both may operate with an AMPC1X Multi-Access Controller, allowing up to four 4500 Central Processors to share the LCS unit.

Each LCS unit is available in one of four storage capacities, as shown on Table 18-1. Models 11-14 are the first LCS unit in a cabinet. Modesl 15-18 are the second unit in a cabinet. Table 18-2 shows Multi-Access options. LCS units operate on 50 Hz or 60 Hz power.

MODEL	WORDS IMPLEMENTED
ALCS11/15	327,680
ALCS12/16	655,360
ALCS13/17	983,040
ALCS14/18	1,310,720

Table 18-1 LCS Options

18.3 PRINCIPAL FEATURES

18.3.1 Access Time

Access time is the time from the program's initiation of an LCS transfer until the addressed sector in the selected LCS track is found, so that the data transfer can begin. The LCS operates as an apparent drum rotating at approximately 2,000,000 RPM, so the average access time is 25 microseconds and the maximum access time is 50 microseconds.

18.3.2 Accuracy

The recoverable error rate for transfers to and from the LCS does not exceed one bit in 10^{11} bits transfered, where a recoverable error is one which can be overcome by accomplishing an error-free transfer within three attempts. The non-recoverable error rate does not exceed one bit in 10^{14} bits.

18.3.3 Transfer Rate

Once an addressed sector is found in an LCS unit, the apparent rotating speed changes to approximately 3810 RPM. The average transfer rate for multiple sector transfers is approximately 162,500 words per second.

18.3.4 Write Protection

A Write Protect selection panel is provided on the LCS unit. It is accessible when the cabinet door is open. Switches on that panel may be used to select 4-track blocks (10,240 words) in the first 32 tracks (81,920 words), and 16-track blocks (40,960 words) for the next 224 tracks, and 128-track blocks (327,680 words) for the balance of the implemented tracks, for protection from inadvertent writing on the selected tracks. When an attempt is made to write on a protected track, a write protect alarm indication is stored in the Alarm Register (18.4.4).

18.3.5 Transferred Data Validity Verification

Each LCS sector (Fig. 18-2) contains a polynomial check segment that contains a unique pattern that is representative of the track number and sector number contained in the header plus the 64 data words. The check segment is generated by the hardware and recorded as the sector is written. The pattern is regenerated by the hardware as the sector is read, and it is compared with the recorded pattern. If they do not compare, a Data Check Alarm (see 18.4.3) is generated. The GENIE Bus data and address parity checking described under 4.5.5 also apply to the Large Core Store Subsystem.

18.3.6 Power Failure Protection

Data recorded in an LCS unit is protected from alteration during power failures or deliberate shutdowns. It is also protected when power is reapplied. Should a power failure occur during a read from the LCS transfer, the Large Core Store Subsystem may sequence off before reading of the sector is completed. Should a power failure occur during a write to the LCS transfer, the integrity of the data and the polynomial check segment may be destroyed. Any transfer interrupted by a power interruption should be reinitiated.

18.3.7 Multi-Access Controller Operation

Operation through the model AMPC10 Multi-Access Controller is identical to operation without multi-port operation unless more than one 4500 Central Processor is requesting access at the same time. When that happens, one is granted access and the others must wait until transfers are completed and access can be granted. A round robin scanner serves each access request in turn to assure that one Central Processor cannot bar access by the others. If access is delayed, the delay time is equal to the transfer time for each previous access granted by the scanner.

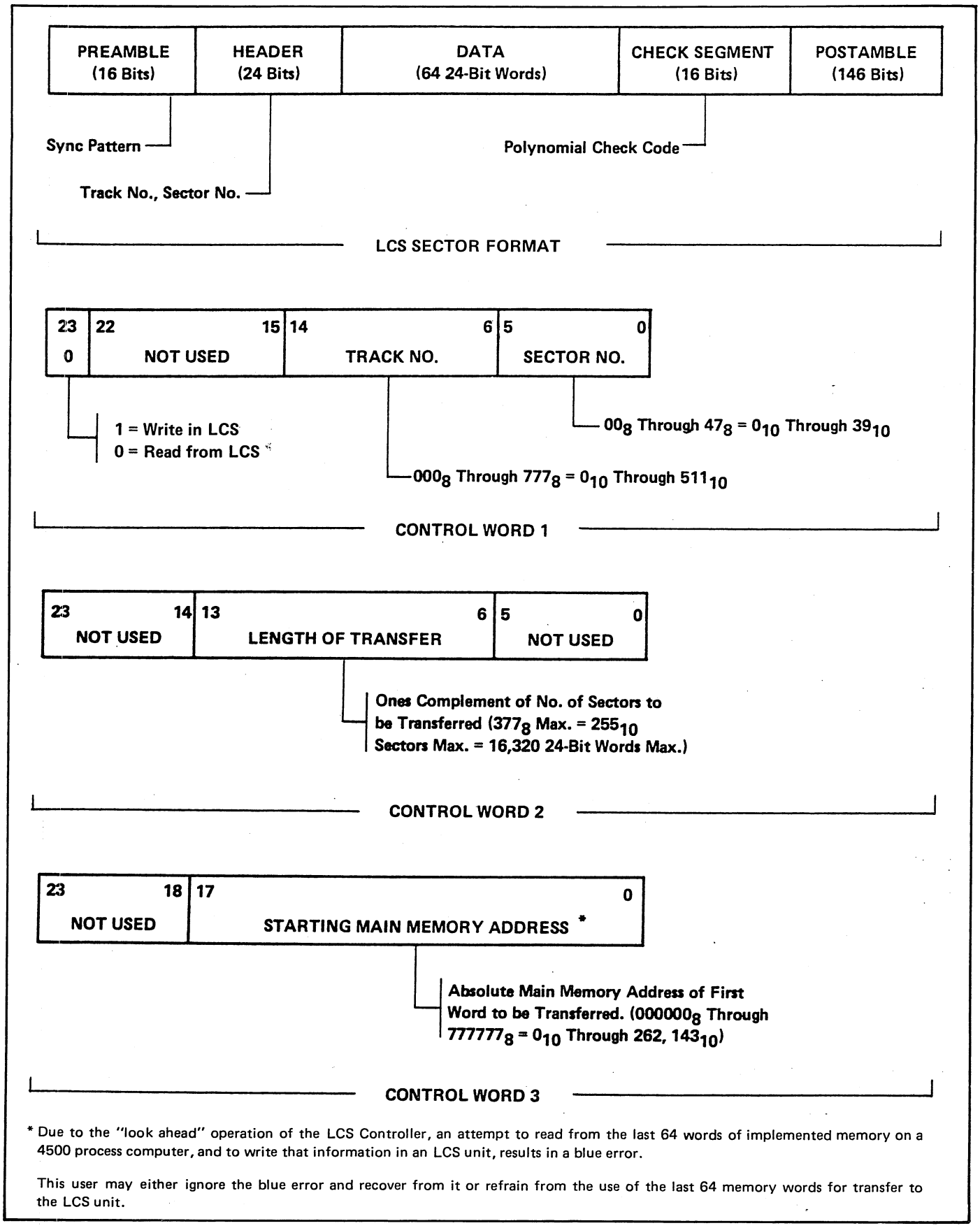
18.4 OPERATING SEQUENCE

The parameters of an LCS transfer are specified by the three control words shown on Fig. 18-2. The control words are transferred to the LCS controller by GEN 2 instructions (18.4.2). Control Word 1, which specifies the starting address in the LCS unit, is transferred from the A Register by an OPR S'=0 instruction addressed to the LCS controller. The OPR S'=0 instruction also initiates the actual transfer. Prior to execution of OPR S'=0, Control Word 2, specifying the length of the transfer, and Control Word 3, specifying the starting main memory address, must have been transferred to the LCS controller. These two words are transferred from the A Register by OUT S'=0 and OUT S'=1, respectively.

18.4.1 Transfer Sequence

The sequence of events in a typical LCS transfer is as follows:

1. The program transfers Control Word 2 and Control Word 3 to the LCS controller by placing each word in the A Register and then executing the appropriate OUT instruction. OUT S'=0 indicates that the word is CW2. OUT S'=1 indicates that the word is CW3. They may be issued in any



* Due to the "look ahead" operation of the LCS Controller, an attempt to read from the last 64 words of implemented memory on a 4500 process computer, and to write that information in an LCS unit, results in a blue error.

This user may either ignore the blue error and recover from it or refrain from the use of the last 64 memory words for transfer to the LCS unit.

Fig. 18-2 LCS Sector and Control Word Formats

order and at any time prior to initiation of the transfer. CW2 is the starting sector address in complemented form (377_8 specifies zero sectors and 000_8 specifies 255 sectors).

2. The program places Control Word 1 in the A Register and executes OPR S'=0 addressed to the LCS controller.

3. The controller goes "not ready", and addresses the track number specified by CW1. When the starting sector address is reached, the transfer begins. As the transfer proceeds, the controller makes necessary main memory requests, updates the main memory and LCS unit addresses, and increments the transfer length count as each full sector is transferred.

4. When the transfer is completed, the drum controller goes "ready" and requests a transfer complete API (18.4.3). The program may then verify that the transfer was error free by executing JNE addressed to the controller.

Should an ABT S'=0 instruction be issued to the LCS controller (18.4.2), or should an error be detected during a transfer (18.4.4), the transfer is completed prematurely, the controller goes "ready", and a transfer complete API (18.4.3) is requested.

Should CW2 specify a transfer of zero sectors, the LCS controller goes "not ready" when OPR is executed, and then "ready", a transfer complete API is requested (18.4.3), and no transfer takes place.

18.4.2 GEN 2 Instructions

The following GEN 2 instructions addressed to the LCS controller affect the Large Core Store Subsystem as described (refer also to 4.5.2):

ABT S'=0; Conditional Abort. This instruction initiates an orderly termination of any LCS controller operation to free the controller for alternate operations. Any operation in progress is terminated as soon as possible without disrupting the integrity of any data movement in progress. If data movement is in progress, the transfer is completed at the end of the current sector.

ABT S'=1; Unconditional Abort. This instruction immediately and unconditionally initializes the LCS controller. It is intended for use in troubleshooting and by test programs, and is not normally used by on-line programs.

ACT; Activate Interrupt. ACT S'=0 activates the transfer complete interrupt and ACT S'=1 activates the unit ready interrupt (see 18.4.3).

AIM; Activate Interrupt Mask. This instruction masks the drum controller transfer complete and unit ready interrupt requests (18.4.3).

DIM; Deactivate Interrupt Mask.

IN Input. IN allows the program to read the contents of the principal LCS controller registers at any time, whether a transfer is in progress or not. If a transfer is in progress or has been completed, the CW1, CW2, and CW3 registers reflect the updating that has taken place since they were set up prior to the transfer. The S' digit in the instruction word indicates which register's contents are to be transferred to the A Register - -

S' = 0 = Alarm Status Register (18.4.4)

S' = 1 = Control Word 1 Register

S' = 2 = Control Word 2 Register

S' = 3 = Control Word 3 Register

JNE; Jump if No Error. This instruction tests the status of the drum controller alarm indicator which is set if any alarm bit in the Alarm Status Register is set (18.4.4).

JNR; Jump if Not Ready. JNR tests the status of the LCS controller "ready" line. The controller is "not ready" from the time a transfer is initiated by OPR until the transfer is complete or terminated prematurely.

OPR; Operate. OPR S' = 0 transfers the contents of the A Register (CW1) to the drum controller and initiates a transfer. CW2 and CW3 should be transferred prior to this transfer request.

OUT; Output. OUT S'=0 transfers Control Word 2 to the drum controller and OUT S' = 1 transfers Control Word 3 to the controller (18.4.1).

18.4.3 Automatic Program Interrupts

At the completion of an LCS transfer or the premature termination of a transfer, the LCS controller requests a transfer complete API. The controller also makes a unit ready (RTZ) API request when a zero length transfer is requested (18.4.1). The unit ready API is provided to preserve a degree of compatibility with programs designed for the dual bulk controller which is used on earlier process computer systems.

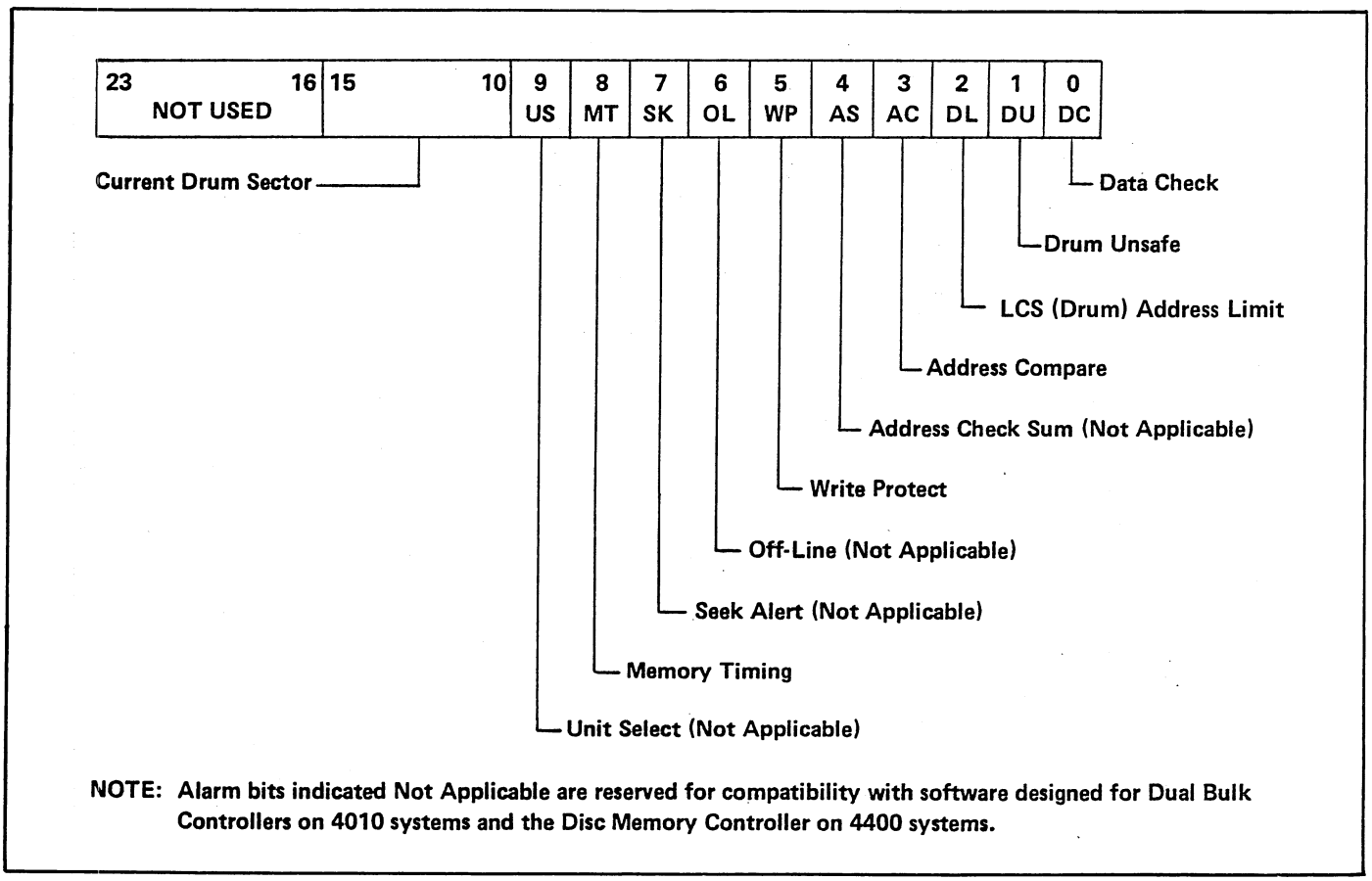
Both API's are inhibitable (4.3.3). The transfer complete API has the higher priority of the two and has the first of the two consecutive interrupt response addresses (4.3.1).

The transfer complete API may also be triggered by ACT S' = 0. The unit ready API may also be triggered by ACT S' = 1 or by OPR S' = 1.

18.4.4 Alarm Detection

The Large Core Store Subsystem hardware detects six alarm conditions that indicate improper hardware or software operation or the inoperability of the hardware. These conditions are indicated by the Alarm Status Register (Fig. 18-3). When any of the alarm conditions is detected, the LCS controller's alarm line, which may be tested by GEN 2 instruction JNE, is set. The Alarm Register may also be transferred to the A Register in the Arithmetic Unit by GEN 2 instruction IN S' = 0. If an alarm is detected while data movement is in progesss, the transfer is completed at the end of the current sector.

The Alarm Register bits and the alarm line are reset (with the possible exception of the DU alarm) when a new transfer is initiated by OPR S' = 0, by the ABT instructions, when the Alarm/Clear button on the Programming and Maintenance Console is pushed, or when the system hardware is initialized.



NOTE: Alarm bits indicated Not Applicable are reserved for compatibility with software designed for Dual Bulk Controllers on 4010 systems and the Disc Memory Controller on 4400 systems.

Fig. 18-3 Alarm Status Register

The alarm conditions are as follows:

Data Check Alarm (DC) (Bit 0). A GENIE Bus parity error has been detected (4.5.5), or on reading from the LCS unit, the polynomial check segment read from the unit did not compare with the check pattern regenerated as the sector was read. If a parity error was detected on the transfer of a control word to the controller, the transfer cannot be initiated until the control word is successfully retransferred. If the alarm occurs while writing on the LCS unit, writing continues to the end of the sector, but the controller writes fill words in the remainder of the sector. If the alarm is due to an incorrect comparison of the check segment, the transfer terminates at that point, which is the end of the sector.

LCS (Drum) Unsafe (DU) (Bit 1). The LCS unit is not ready for operation, either because its power supply is out of tolerance or because both read and write control signals are being applied to the unit at the same time.

LCS (Drum) Address Limit (DL) (Bit 2). The LCS unit address specified by the controller exceeded the highest address implemented in the unit. This could be due to an incorrect Control Word 1, a transfer beginning at an implemented address but continuing beyond the highest implemented address, or a hardware failure.

Address Comparison Alarm (AC) (Bit 3). On a read from the LCS unit transfer, the address read from the sector header did not compare with the address in the LCS controller's address (CW1) Register. As transfers proceed, the address register is incremented as each sector boundary is reached. If the address read from a sector does not compare with the controller's address register, either an incorrect first sector for a transfer was found, or during the transfer, the controller and the LCS did not maintain the same sector sequence.

Write Protect Alarm (WP) (Bit 5). An attempt was made to write on an LCS unit track protected by the Write Protect selection switches (18.3.5). This can be due to a software error, incorrect selection of a Write Protect switch, or a hardware malfunction.

Memory Timing Alarm (MT) (Bit 8). A request for main memory access was not honored before a data word read from the LCS unit was replaced by a new word read from the unit, or was not honored in time to provide a new word to be written on the drum. This alarm could occur because of a hardware malfunction or because DMA activity on the GENIE Bus is so high that the memory data bandwidth of the bus is exceeded. The bus memory data bandwidth could be exceeded due to a large number of devices on the bus with DMA capability and the occurrence of a period of high DMA demand.

18.5 ADDITIONAL LCS SUBSYSTEM CHARACTERISTICS

18.5.1 Primary LCS Cabinet Power

The auxiliary cabinet in which an LCS unit is installed may be supplied 115 Vac ±10% power at either 50 Hz or 60 Hz.

18.5.2 LCS Cabinet Physical Characteristics

The LCS cabinet is 30" wide, 76" high, and 32" deep. The cabinet weighs approximately 300 lbs.

18.5.3 Environmental Classes

The LCS controller and the LCS unit are in environmental class A. See 3.1 and Table 3-1.

Model	Ports Provided
AMPC11	One
AMPC12	Two
AMPC13	Three
AMPC14	Four

Table 18-2 Multi-Access Options

ANALOG INPUT SUBSYSTEM DEFINITION OF TERMS

The following statements define the terms used in describing the model APIA1 Analog Input subsystem performance in section 12 of this manual. Refer to the TDC 7100 General Description for systems using the Data Hiway Interface.

1. System Performance

The term system performance contained herein pertains only to the analog signal relationships as described below:

a. Analog Inputs

The performance described specifies the analog relationship from the multiplexer input terminals (S +, S -) to the A/D Converter output. The digital code for the A/D Converter is true binary for positive voltages at the multiplexer input and 2's complement for negative voltages when referenced at the A/D Converter output.

b. Variable Outputs

The performance described specifies the relationships from the digital code at the input of the D/A Converter to the analog output located at the VOC output multiplexer terminals.

c. Absolute Analog Outputs

The performance described specifies the relationship from the digital code input of the AAO generator output terminals.

2. Scan Rate

Scan rate is defined as the maximum random scan rate the system is capable of, in points per second. Some degradation in performance may occur if a single point is scanned more than once per second.

3. Repetitive Scan Rate

Repetitive scan rate is defined as the maximum rate at any one point may be scanned.

4. Full Range

Full range is defined as the algebraic difference between the minimum and maximum values to which the Analog Input/Output subsystem is specified.

Example

Specification	Full Range
$\pm$10 mV	20 mV
-10 mV to +50 mV	60 mV

5. Gain Error

Gain error is defined as the deviation of the mean of a normal or Gaussian distribution from the actual value. Gain error is specified in % FR and as an error which is gain dependent. When measuring gain error, proper offset techniques must be applied. Gain error is specified at 25° C $\pm$3°C and the proper gain error coefficient must be taken into account as the temperature deviates from this range. When measuring gain error using Hg relay multiplexers for analog inputs, the maximum repetitive scan rate is one point/second.

6. Repeatability Error

The graph of Fig. A-1 describes a Gaussian distribution of count values about the mean count value $\overline{X}$. $\overline{X}$ is calculated by taking N samples and then averaging them. Repeatability error is expressed as a plus and minus three sigma deviation from the mean, $\overline{X}$. Three σ means that for a normal distribution 99.7% of all readings are within this $\pm 3\ \sigma$ range. In terms of evaluation of the analog subsystems, $\pm 3\ \sigma$ specifies that 0.3% of N readings may be disregarded. The readings to be disregarded are the readings furthest from the mean. Repeatability error is expressed as a percentage of full range.

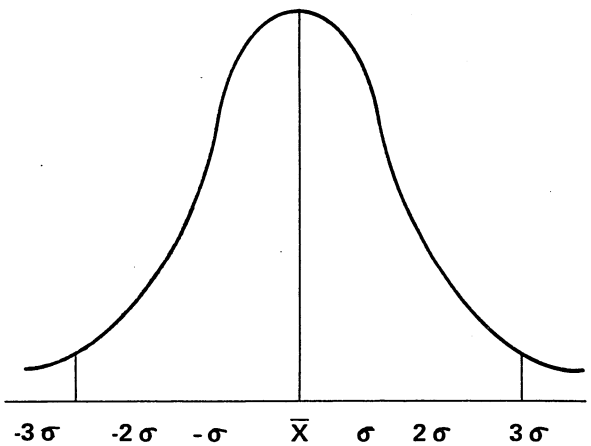


Fig. A-1 Frequency Distribution of Count Values - Gaussian Curve

7. Common Mode Voltage

The voltage at both the S+ and S- terminals can be raised above and below the system logic ground. Common mode voltage is defined as the voltage with respect to system logic ground that these inputs may be raised while the system still processes the differential input signal. The Maximum Common Mode Voltage is the sum of the common mode voltage plus the signal voltage when referenced in this specification.

8. Common Mode Rejection

The common mode rejection of the analog input subsystem is defined as the ability of the system to reject a signal that is common to both differential inputs (S+, S-) with a source unbalance of 100 ohms or less. Proper signal conditioning must be used when making this measurement (60 db filters). The CMR is specified from dc to 60 Hz ac and in db.

9. Crosstalk

Crosstalk effects are defined as the errors created by signal or common mode voltages from one point into or affecting the point being measured. Crosstalk is specified in terms of the ability of the system to reject these signals from the point being measured from dc to 60 Hz.

10. Offset

Offset is defined as the magnitude of the output when the input is zero. When measuring gain error, repeatability error, CMRR, and crosstalk, proper offset techniques must be applied.

11. RTI (Referred to the Amplifiers Inputs)

An error that has an RTI contribution is gain dependent.

An example is:

GE = ±0.025% FR ±10 uV RTI

To convert the 10 uV RTI affect in terms of FR, refer to the table below:

System Gain	FR	%FR	Total GE (%FR)
1000	20 mV	.05	.075
500	40 mV	.025	.05
250	80 mV	.0125	.0375

Where:

$$\% \text{ FR} = \frac{10 \text{ uV}}{\text{FR}} \text{ X } 100$$

DIGITAL PROCESS INTERFACE (DPI) MODULES APPLICATION INFORMATION

INTRODUCTION

This document defines unique software application characteristics of the various types of interface modules used in the model APID1 Digital Process Interface (DPI) subsystem. Specifically, this document identifies the "Z" bits, data formats and sequences, and the clip options affecting software for the modules. It does not describe the unique characteristics of the operating system driver for this subsystem, since that information is contained in the corresponding design specification and RTMOS Application Manual.

This document is divided into two main sections: Part I, which provides general definition of the categories of information covered within this document; and Part II, which contains reference tables and descriptions to provide detailed information by module category.

Included in this document are cross references to information contained in the DPI's general description, located within the main body of the General Description publication, and cross references between tables and descriptions within this specific appendix document.

"Z" Bits

"Z" bits are used by the DPI subsystem to provide additional microcode control of interface modules, where required. Depending upon the module type, they may be used for such purposes as directing selective input/output transfers, for general clearing of termination assembly modules, for selective clearing of modules or circuits within a module, or for extending data fields.

Some of the interface module categories do not require the use of "Z" bits to supplement the command byte when defining the operation. Specifically, filter inputs require only the command byte, indicating a read operation. Similarly, latching/momentary (but not confirmed) outputs and digital display drivers do not require "Z" bits; their operation is defined simply by indicating a write operation in the command byte. Modules not requiring "Z" bits can be operated with "Z" bits, if certain conventions are followed, as indicated below:

Inputs

Z3 must equal logic 1 or a Device Unavailable (DU) indication will occur. Z2 and Z1 will have no effect, unless Z3 is a logic 0, which will result in a DU indication.

Outputs

Z2 must equal logic 1 or a Device Unavailable (DU) indication will occur. Z3 and Z1 will have no effect.

Tables B-1, B-2, and B-3 include a column, "Z Bits Required?", that indicates whether or not "Z" bits are required by the various module categories. If the column indicates that "Z" bits are not required, it provides an indication of the type of command operation needed. If the column indicates that "Z" bits are required, it provides a reference to a description later in this document.

Data Formats and Sequences

The number, format and sequence of data transfers required for the various types of interface modules are defined by the subsequent "Z" bit and data format descriptions. Contrasting examples of these requirements are the filter inputs and analog inputs. A single filter input module's eight-circuit status can be obtained by a single input call, but an analog input's single-circuit status requires a call to initiate the A/D conversion and then two input calls to read the converted value.

Interrupts

Interrupt indications from termination assemblies will occur in either a sequence-of-events or a non-sequence-of-events (also referred to as "change detect") mode. The sequence-of-events mode requires all interface modules within the termination assembly to be change detect. The non-sequence-of-events mode is used where there are either interrupt modules that are not change detect or there is a mixture of change detect modules with other interrupt or non-interrupt categories. An example of an interrupt module category other than change detect is the console lamp driver module which has an interrupt associated with

its keyboard input function. (Refer to the RTMOS Application Manual for response differences between the sequence-of-events modes.)

Non-sequence-of-events interrupts can be assigned to either class I or class II interrupt categories by pin selection at the individual modules. If assigned class I, the interrupts will be identified in the interrupt status information passed to the user as one of eight modules within one-half of a termination assembly. If assigned to class II, the interrupt will be specifically identified within the assembly. (Class I is normally not used.)

Status Word

An eight-bit controller status word is obtained by the TDC 4500 RTMOS Operating System following each data or interrupt transfer operation. This status word contains information relating to interrupt and data transfer operations handled by the controller. The significance of the individual status word bits containing this information is described within the "Status Check" portion of the DPI's general description, provided within the main body of this publication.

The status words are examined by the operating system following a call. The operating system will attempt retries on certain conditions and will call up a corrective action subroutine if the retries are unsuccessful. Refer to the RTMOS Application Manual for details on status checks and corrective action.

> NOTE
>
> The interrupt-related bits of the status word are masked by the operating system when the status word is passed to the user.

Refer to "Application Information", in the Digital I/O Controller FDS, drawing no. 70A126725 for further assistance in interpretation of status responses from the DPI's controller.

"Z" BIT AND DATA FORMAT REFERENCES

The following information is divided into three general categories of interface modules: Input, Output, and Console. Each category includes several types of modules and provides specific information pertaining to that category. The specific information provided for each module type is covered under the headings of "Z" Bit Formatting (A), User Call "Z" Bits and Data Formats (B), and, where applicable, Pin Options Affecting Software (C). These headings are cross referenced from Tables B-1, B-2, and B-3.

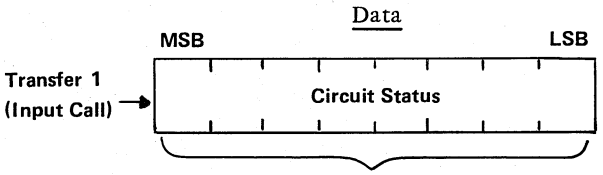
Input Modules

① Filter Inputs (8/Module)

A. Z Bits Formatting

Z bits not required.

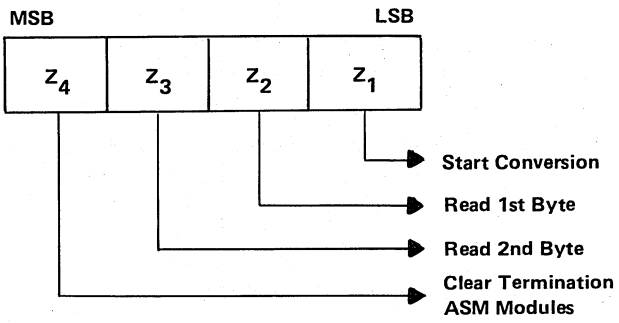
B. User Call Z Bits and Data Formats



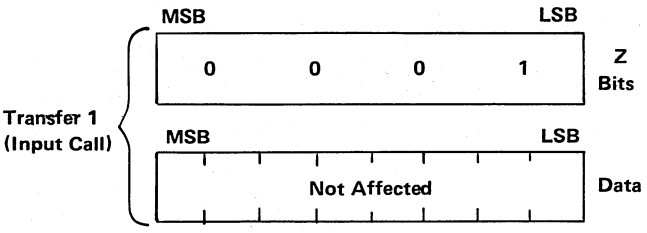
Logical "1" in bit positions indicates corresponding circuit closed; logical "0", circuit open. (T^2L modules, ICFH1 and ICDH1, provide inverse indications - i.e.: "1" = ckt. open, "0" = ckt. closed.)

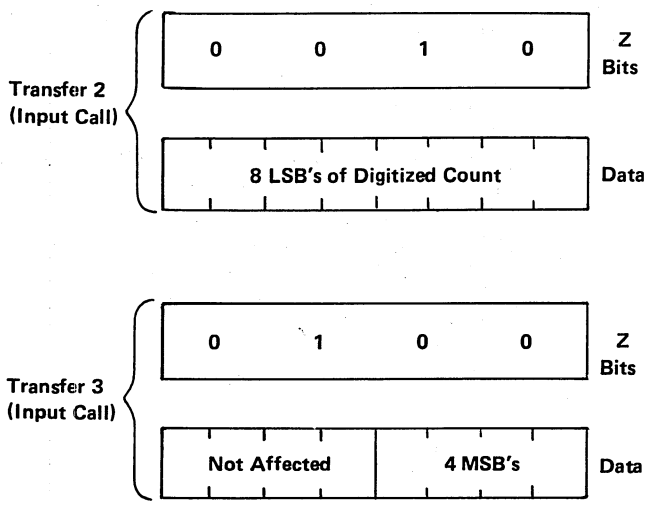
② Analog Inputs (1/Module)

A. Z Bit Formatting: (Z Bits Required)



B. User Call Z Bit and Data Formats





C. Pin Options Affecting Software

1. Binary /2's Complement

The format of the 12-bit digitized count input in the 2 byte transfer will be either binary or 2's complement as selected by pin jumper on the module. Refer to Table B-4 for the binary format and to Table B-5 for the 2's complement.

2. Pin Select Ranges

This mode can be set to one of three ranges by pin selection. The three ranges are:

a. ±5 V

b. ±10 V

c. 0 V to 10 V

The range selected determines the value of the individual bits in the 12-bit count. See the following tables to determine the correspondence of values per bit/range:

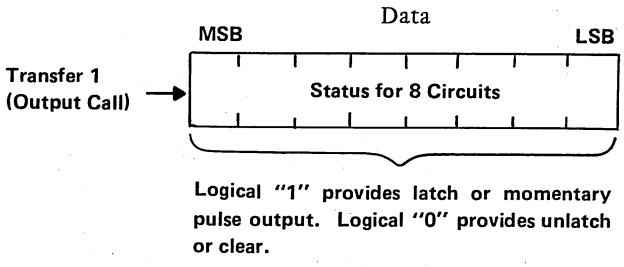
±5 V, ±10 V, 0 V to 10 V
(Table B-6)

Output Modules

① **Latching/Momentary Relays - Form "A", "B"**
(8/Module)

A. Z Bits not required

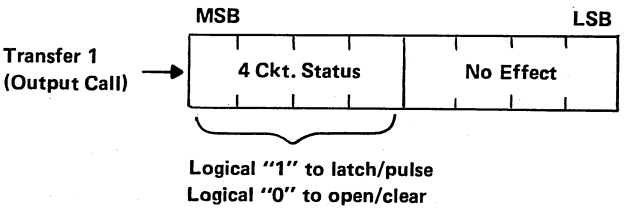
B. User Call Z Bit and Data Formats



② **Latching/Momentary Relays - Form "C", "D"**
(4/Module)

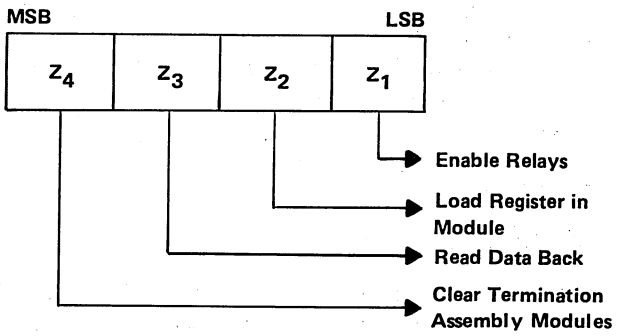
A. Z Bits not required

B. User Call Z Bit and Data Formats

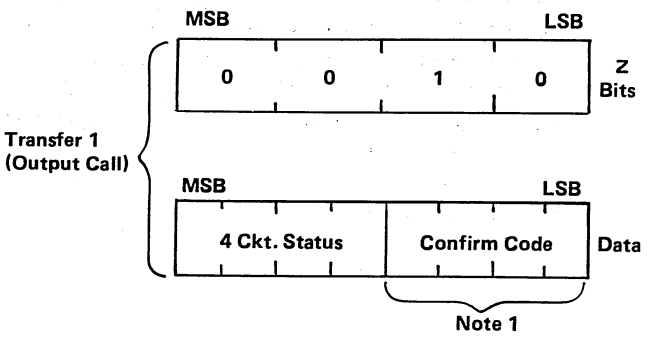


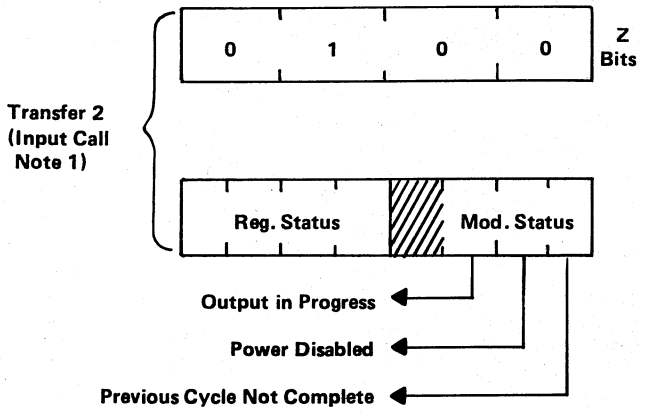
③ **Confirmed Outputs** (4/Module)

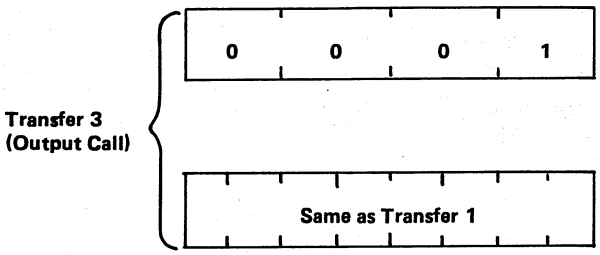
A. Z Bit Formatting (Z Bits Required)



B. User Call Z Bit and Data Formats







NOTES:

1. Confirm code must correspond to that pin selected on module, If not, device unavailable error occurs.

2. Transfer 2 may be circumvented. Only Transfers 1 and 3 required for operation. Transfer 2 provides optional capability for comparison of output data with that readback from module's register.

C. Pin Options Affecting Software

1. Confirmed/Latching

The confirmed output modules contain a pin option that enables their usage as either confirmed outputs or normal latched outputs. If selected as confirmed outputs, they require two output transfers to perform the operation and can also respond to an input read status transfer. The first of the two output transfers contain four bits to indicate the desired output status and four bits of a confirm code. (See item 2, Confirm Code.) The second of the output transfers enables the actual output function according to the information provided in the first transfer.

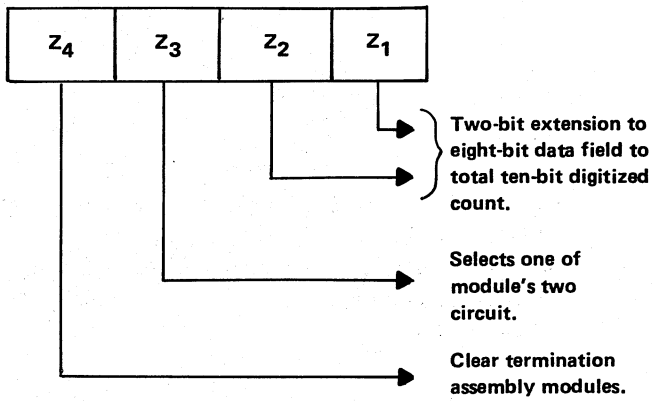
If the confirmed output module is pin selected as a standard latching output, it functions the same as a Form "C" latching output, as described by item (2) of the Output Modules.

2. Confirm Code

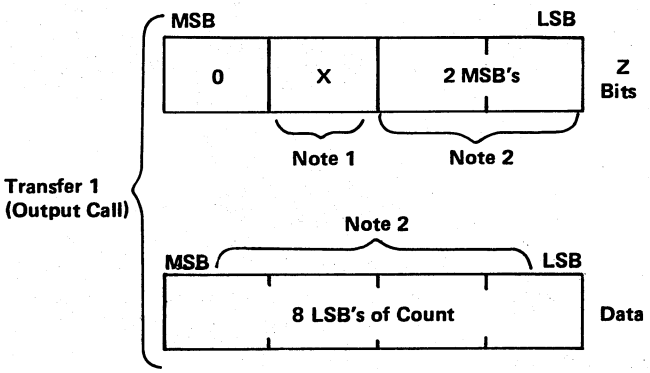
When selected by pin option as a confirmed output, the module must have a confirm code pin selected. The four LSB's of the first output transfer must match this pin-selected code.

(4) **10-Bit Analog Outputs** (2/Module)

A. Z Bit Formatting (Required for operation)



B. User Call Z Bit and Data Formats



NOTES:

1. X = "0" or "1" to select one of two circuits.

2. Binary format for unipolar modified 2's complement for bipolar. (See Table B-7 for voltage outputs. See Table B-8 for current outputs.)

C. Pin Options Affecting Software

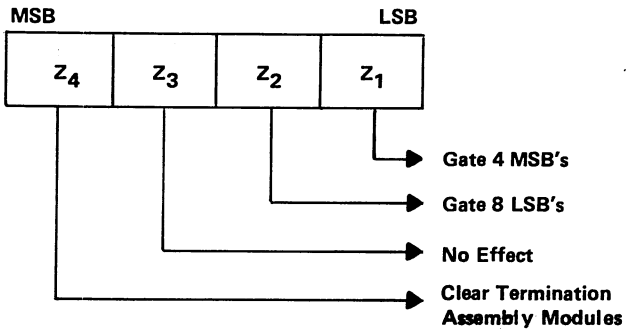
1. Ranges

The 10-bit analog voltage output modules have three pin-selectable output voltage ranges: ±5 V, ±10 V, and 0 V to 10 V. The specific range selected at the module will determine the output data format. Although all output data codes to represent an analog output are 10 bit, their format and value significance are a function of the range selected.

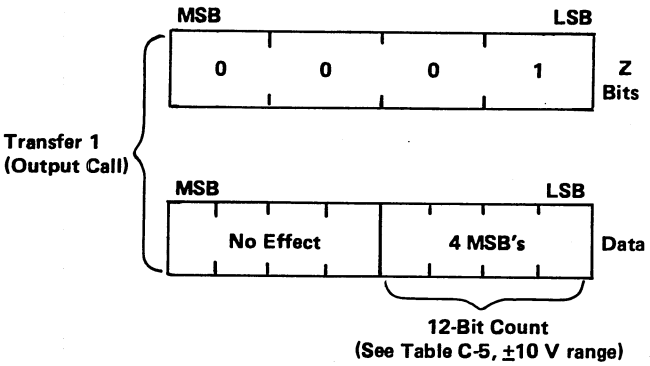
Table B-9 provides the format and bit significance for ±5 V, ±10 V, and 0 V to 10 V ranges.

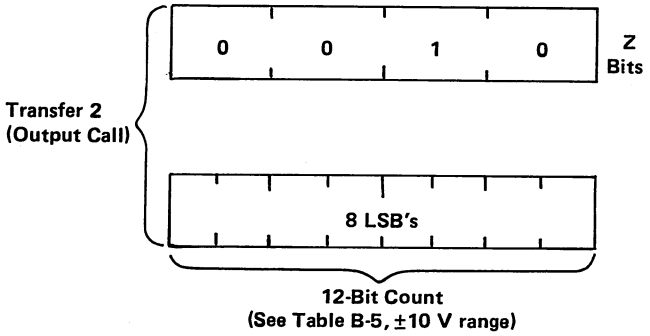
⑤ **12-Bit Analog Outputs** (1/Module)

A. Z Bit Formatting (Required for operation)



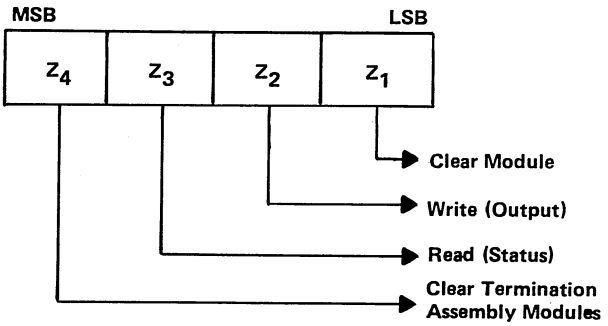
B. User Call Z Bit and Data Format





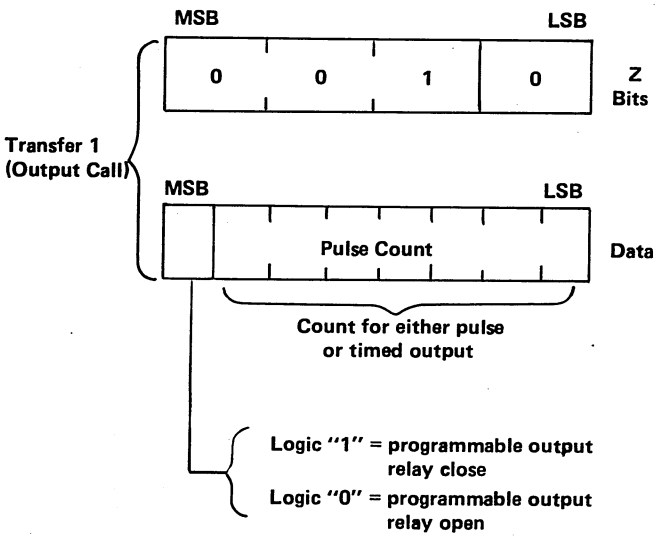
⑥ **Programmed Pulse Train Generator**
(Pulse Train or Timed Output)

A. Z Bit Formatting

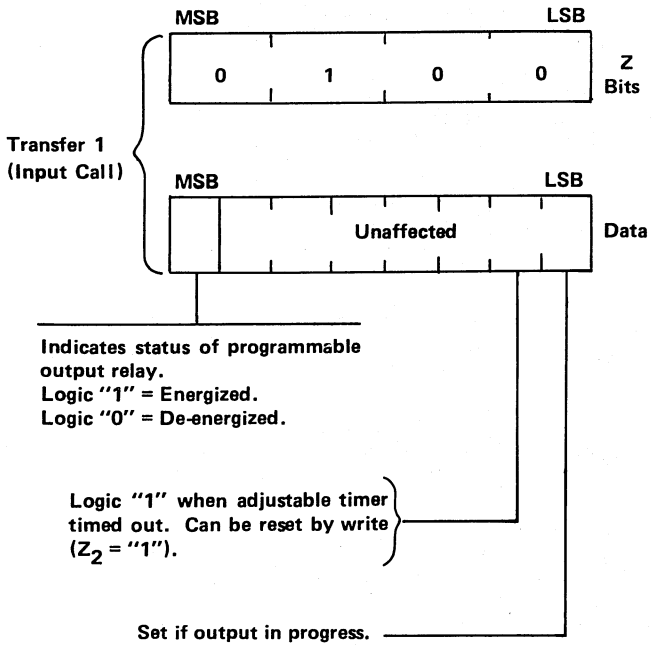


B. User Call Z Bit and Data Formats

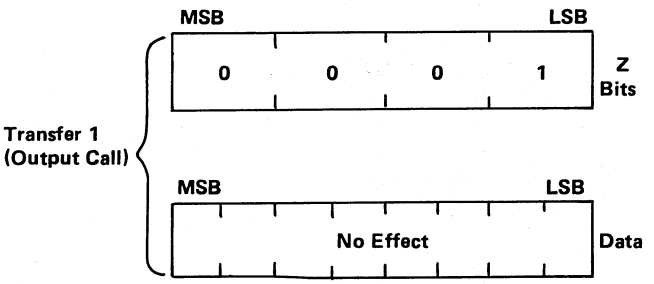
1. To output timed output status or pulse train count.



2. To read status from module.



3. To clear pulse train or timed output.



The clear operation terminates any output in progress and clears any existing error condition.

C. Clip Options Affecting Software

1. Class I/Class II/Disable Interrupts

This pin option is used to select one of three interrupt modes for the module. The disable mode prevents recognition of an interrupt. The class 1 and class II modes both enable detection of the interrupt, but differ in the indication given to the termination assembly control for transfer during controller polling operations. If pinned for class I, the interrupt status made available for the operating system will indicate only that the interrupt occurred in one of eight modules within an assembly. If pinned for class II, it will provide status that indicates the specific module where the interrupt occurred.

The interrupt, if enabled, indicates that either a normal completion or deadman timeout condition occurred. A normal completion is when either the desired number of pulses have been generated or the desired timed output period has occurred, as indicated by a completed countdown of the count specified.

2. Enable/Disable Deadman

This pin option is used to either enable or disable the adjustable deadman timeout circuit. The timeout circuit, when enabled, is used to provide an indication if a normal output operation does not complete in a time interval shorter than that adjusted for the circuit.

3. Pulse/Timed Output

This clip option is used to specify the module's function as either a pulse generator or a timed output.

4. Output Clock Frequency

Clock increments of 8, 16, 32, 64, or 128 ms are available by pin selection to be used in counting down timed output count. The timed output operation will be a function of the output count and the clock frequency selected.

(7) Solid State Latches

A. Z Bit Formatting - None

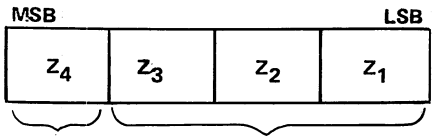
B. Each bit set in the output byte closes the corresponding solid state latch. Each bit reset opens the corresponding latch.

C. Clip Options Affecting Software - None

Console Modules

① Lamp Drivers

A. Z Bit Formatting (Required for operation)

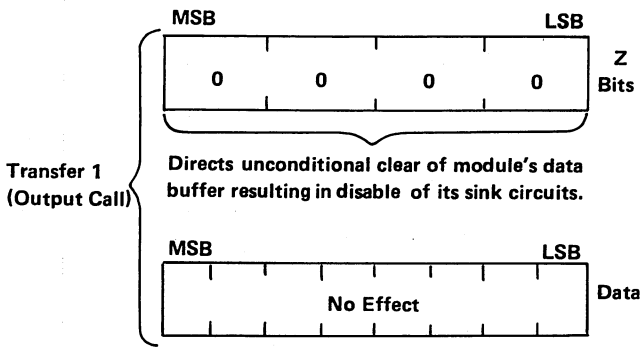


Clear Term. Asm. Modules

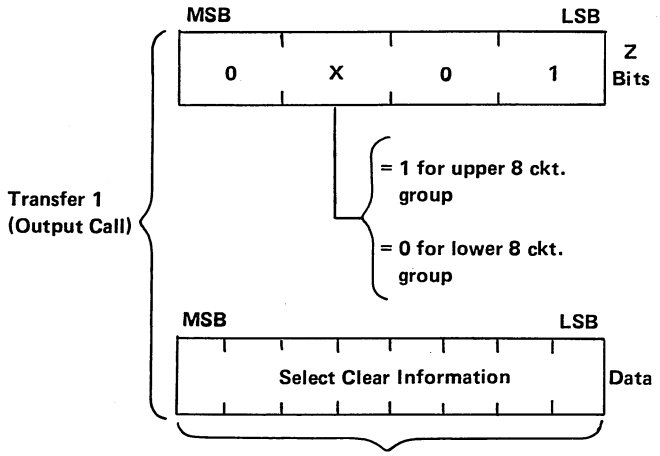
Z_3	Z_2	Z_1	
0	0	0	Clear (All Bits)
0	0	1	Selective Clear (8 MSB's)
0	1	0	Selective On (8 MSB's)
0	1	1	Selective Flash (8 MSB's)
1	0	1	Selective Clear (8 LSB's)
1	1	0	Selective On (8 LSB's)
1	1	1	Selective Flash (8 LSB's)

B. User Call Z Bit and Data Formats

1. Clear all module driver circuits.

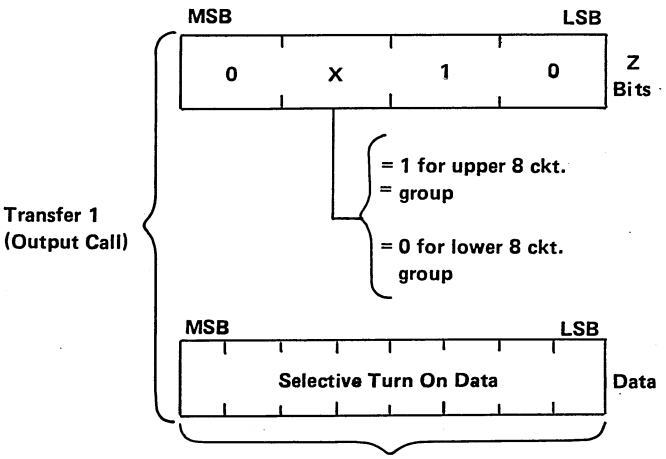


2. Selective clearing of module's driver circuits.



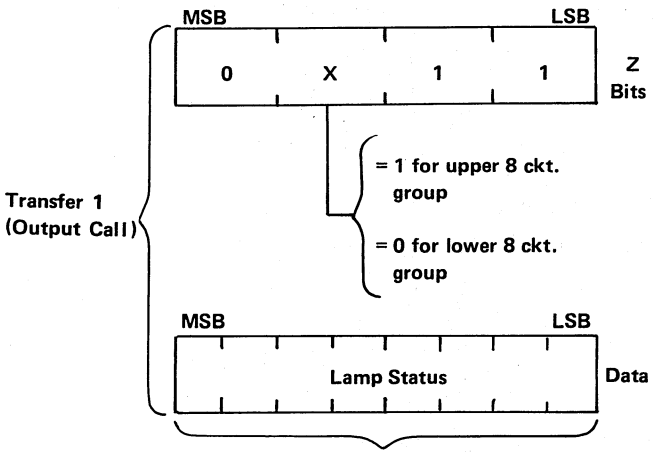
Logic "1" in bit position specifies clearing of the corresponding lamp's sink circuit. Logic "0" does not affect the corresponding circuit.

3. Selective turn on of module's driver circuits.



Logic "1" in bit position specifies turn on of the corresponding lamp's sink circuit. Logic "0" does not affect the corresponding circuit.

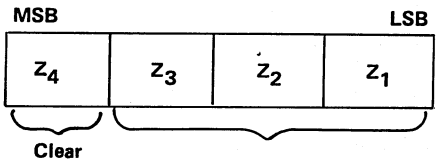
4. Selective flash of module's driver circuits.



Logic "1" in bit position specifies flash of the corresponding lamp circuit. Logic "0" does not affect the corresponding circuit.

(2) Console Lamp Drivers

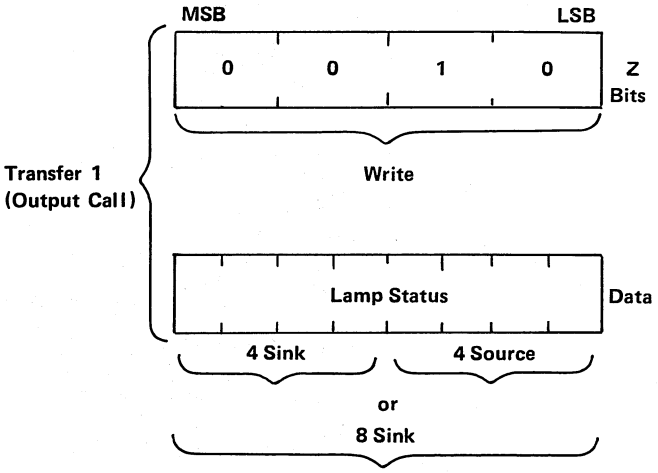
A. Z Bit Formatting (Required for operation)



Z_3	Z_2	Z_1	
0	1	0	Write (Output)
0	1	1	Select Clear
1	0	0	Read, No Clear
1	0	1	Read, Unconditional Clear

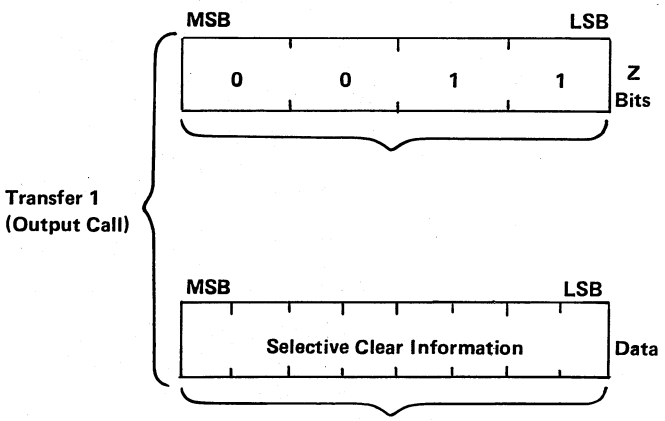
B. User Call Z Bit and Data Formats

1. To output to lamp drivers.



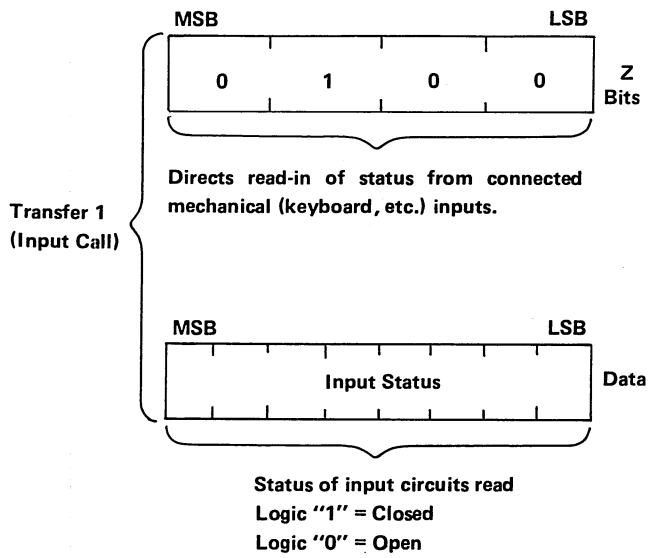
Pin option on module can be set to specify code in either 4 by 4 matrix, permitting selection of one of up to 16 circuits, or in a straight 8-bit selection to select one of up to 8 circuits.

2. To selectively clear circuits.

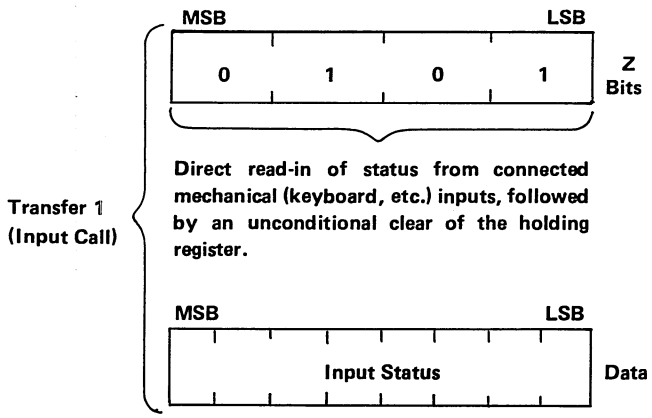


Logic "1"s specify clearing of respective circuit. Logic "0"s have no effect.

3. To read, without clearing, keyboard inputs.



4. Unconditionally clear lamp driver source/sink circuits.



C. Clip Options Affecting Software

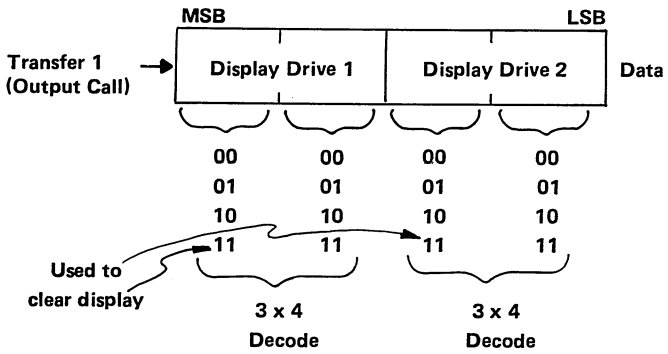
1. Inhibit/Enable API's.

Four pin jumpers are available to either enable or disable interrupts from keyboard input contacts connected to this module for read-in. These clips enable or disable API's for inputs associated with the four LSB's only.

③ **Digital Display Drivers** (2/Module)

A. Z Bits Not Required

B. User Call Z Bit and Data Formats



④ **Keyboard Encoder**

This module is not driven directly by the controller. It typically interfaces through a console lamp driver module, via its input capability. The keyboard encoder module converts input select information to binary coded output, which is transferred to a holding register in the console lamp driver module. (Refer to "Console Modules - Console Lamp Drivers, item 3" for instructions on formatting.)

A. Clip Options Affecting Software

1. X/Y Encoding Options

These clip options establish binary coding by either mode "X" or mode "y", as defined below:

X Mode

Two codes - one three bit, one of seven; and one five bit, one of 23.

Y Mode

Two codes - each four bits long, encoding one of 15.

	MODULE TYPE (PX3650___)	FUNCTION	CLIP OPTIONS	CLIP OPTION AFFECT SOFTWARE?		Z BIT AND DATA FORMAT REFERENCES (NOTE 2)	Z BITS REQUIRED?		
				YES (NOTE 1)	NO		YES	NO	HOW OPERATED? (NOTE 3)
FILTER INPUTS: ICF– IOI–	ICFH1	100 ns delay TTL Contact Filter Input	Pwr/125 V Stor	–	X	See Input Modules, – Item ①, Filter Inputs.	–	X	READ
	ICFH2 ICFI2 ICFJ2	.1 ms 1 ms 28 V Contact Filters 22 ms	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
	ICFH3 ICFI3 ICFJ3	.1 ms 1 ms 48 V Contact Filters 22 ms	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
	IOII1 IOIK2 IOIJ2	1 ms 4 ms 28 V Block Isolated 22 ms Contact Filters	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
	IOIL2 IOIM2 IOIN2	1 ms 4 ms 28 V Point Isolated 22 ms Contact Filters	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
	IOII3 IOIK3 IOIJ3	1 ms 4 ms 48 V Block Isolated 22 ms	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
	IOIL3 IOIM3 IOIN3	1 ms 4 ms 48 V Point Isolated 22 ms Contact Filters	Pwr/125 V Stor (To Enable/Disable 125 V Buffering)	–	X	"	–	X	"
CHANGE DETECT INPUTS: ICD– IED–	ICDH1	100 ns delay TTL Contact Change Detect Input	1. INT1/INT2 2. Disable/Acknowledge 3. Pwr/125 V Stor	X X –	– – X	See Input Modules – Item ① Filter Inputs.	–	X	"
	ICDH2 ICDI2 ICDJ2	.1 ms 1 ms 28 V Contact Change 22 ms Detect	1. INT1/INT2 2. Disable/Acknowledge 3. Pwr/125V Stor	X X –	– – X	"	–	X	"
	ICDH3 ICDI3 ICDJ3	.1 ms 1 ms 48 V Contact Change 22 ms Detect	1. INT1/INT2 2. Disable/Acknowledge 3. Pwr/125 V Stor	– X –	X – X	"	–	X	"
	IEDI2 IEDK2 IEDJ2	1 ms 28 V Contact Change 4 ms Detect with Block 22 ms Isolation	1. Edge Detection 2. Pwr/Stor 3. INT1/INT2	X – X	– X –	"	–	X	"
	IEDL2 IEDM2 IEDN2	1 ms 28 V Contact Change 4 ms Detect with Point 22 ms Isolation	1. Edge Detection 2. Pwr/Stor 3. INT1/INT2	X – X	– X –	"	–	X	"
	IEDI3 IEDK3 IEDJ3	1 ms 48 V Contact Change 4 ms Detect with Block 22 ms Isolation	1. Edge Detection 2. Pwr/Stor 3. INT1/INT2	X – X	– X –	"	–	X	"
	IEDL3 IEDM3 IEDN3	1 ms 48 V Contact Change 4 ms Detect with Point 22 ms Isolation	1. Edge Detection 2. Pwr/Stor 3. INT1/INT2	X – X	– X –	"	–	X	"
125 V INPUT BUFFER IPI– IBI–	IBIA1	Block Isolation Buffers 125 V to 28 V	–			Transparent to Info.	–	X	"
	IPIA1	Point Isolation Buffers 125 V to 28 V	–			"	–	X	"
ANALOG INPUTS	IADA1	Analog to Digital Converter	1. Binary or 2' complement 2. Isolation/Non-Isolation 3. Pin-Select Ranges	X – X	– X –	See Input Modules – Item ②, Analog Inputs	X	–	

NOTES:
1. See category C, "Clip Options Affecting Software", within the individual module category descriptions.
2. See categories A and B, "Z Bit Formatting" and "User Call Z Bit and Data Formats", within the individual module category descriptions.
3. See "Z Bits" in Introduction.

Table B-1 Input Module Categories

	MODULE TYPE (PX3650__)	FUNCTION	CLIP OPTIONS	CLIP OPTION AFFECT SOFTWARE?		Z BIT AND DATA FORMAT REFERENCES (NOTE 2)	Z BITS REQUIRED?		
				YES (NOTE 1)	NO		YES	NO	HOW OPERATED? (NOTE 3)
Latching Outputs IHB –	IHBA3 IHBD2 IHBE2	250 VA, Form "D" 100 VA, Form "A" 100 VA, Form "B"	+28 V/+12 V Pwr	–	X	Output Modules – Form "A", "B" – Item ① Form "D" – Item ②		X	→ Write
Momentary Outputs IHS	IHSD1 IHSD2 IHSB3 IHSE2	100 VA, Form "A" 100 VA, Form "A" 250 VA, Form "D" 100 VA, Form "B"	1. +28 V/+12 V Pwr 2. Count Select 3. Clock Select 4. Latched/Momentary	– – – –	X X X X	"		X	→ Write
Confirmed Outputs IHC –	IHCO1	100 VA, Form "C"	1. Data Confirmation Pattern 2. Relay Power 3. Confirmed/Latch 4. Energize Period	X – X –	– X – X	Output Modules – Confirmed Outputs, Item ③ ←	X	–	
D/A Converters (Current) IDAA –	IDAA1 IDAA2 IDAA3 IDAA4	Converts binary or modified 2's complement 10-bit code to current output	Isolation/Non-isolation	–	X	Output Modules – Analog Outputs, Item ④ ←	X	–	
D/A Converters (Voltage) IDAV –	IDAV1	Converts binary or modified 2's complement 10-bit code to voltage output	1. Isolation/Non-isolation 2. Ranges	– X	X –	" ←	X	–	
Programmed Pulse Train Generator PPTG –	PPTG1	Pulse train timed output	1. Class I/II Interrupts 2. Pulse/Timed Output 3. Output Clock Frequency 4. Enable/Disable Deadman	X X X X	– – – –	Output Modules – Programmed Pulse Train Generator, Item ⑥ ←	X	–	
D/A Converter (Voltage) IDAB –	IDAB2	Converts 2's complement 12-bit binary code to bipolar (±10 V) voltage output	Isolation/Non-isolation	–	X	Output Modules – 12-bit analog outputs, Item ⑤ ←	X	–	
Solid State Latches	ISSO1	50 V open max., 500 mA closed max.	None		X	Item ⑦		X	→ Write

Table B-2 Output Module Categories

	MODULE TYPE (PX3650__)	FUNCTION	CLIP OPTIONS	CLIP OPTION AFFECT SOFTWARE?		Z BIT AND DATA FORMAT REFERENCES (NOTE 2)	Z BITS REQUIRED?		
				YES (NOTE 1)	NO		YES	NO	HOW OPERATED? (NOTE 3)
Lamp Drivers ILDA –	ILDA1 ILDA2	Provides selective On/Off/Flash of up to 16 lamps	1. Warm/Stor 2. +12 V/+28 V Pwr	– –	X X	See Console Modules – Item ①, Lamp Drivers	X X	– –	
Console Lamp Drivers ICLA –	ICLA1 ICLA2	Provides individual or group (8) Control of Lamp Driver Circuits. Includes Readback.	1. Sink/Source 2. +12 V for source 3. Enable/Disable API	– – X	X X –	See Console Modules – Item ②, Console Lamp Drivers.	X	–	
Digital Display IDDC –	IDDC1 IDDC2	Provides drive for two Digital Display Circuits	1. Local/Remote Pwr	–	X	See Console Modules – Item ③, Digital Display Drivers.	–	X	→ Write
Keyboard Encoders IKEA –	IKEA1	Provides encoded binary value in response to switch selections	1. "X"/"Y" Encoding options	X	–	See Console Modules – Item ④, Keyboard Encoder.	–	X	Read →

NOTES: See Table B-1.

Table B-3 Console Module Categories

SAMPLE RANGE POINTS	CODE FOR RANGE POINTS											
	MSB	MSB -1	MSB -2	MSB -3	MSB -4	MSB -5	MSB -6	MSB -7	MSB -8	MSB -9	MSB -10	LSB
F.S. – 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1
+3/4 F.S.	1	1	0	0	0	0	0	0	0	0	0	0
+1/2 F.S.	1	0	0	0	0	0	0	0	0	0	0	0
+1/4 F.S.	0	1	0	0	0	0	0	0	0	0	0	0
0 V + 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1
0 V	0	0	0	0	0	0	0	0	0	0	0	0

Table for 12-bit D/A output or A/D input in 0 V to 10 V range

NOTES:

(1) F.S. is full scale. Full count (all "ones") yields F.S. - 1 LSB.

(2) MSB is most significant bit. LSB is least significant bit. (See Table B-6 for voltage value per bit position.)

Table B-4 12-Bit, Unipolar (0 V to 10 V) Analog (D/A or A/D)

SAMPLE RANGE POINTS	CODE FOR RANGE POINTS											
	MSB	MSB -1	MSB -2	MSB -3	MSB -4	MSB -5	MSB -6	MSB -7	MSB -8	MSB -9	MSB -10	LSB
F.S. - 1 LSB	0	1	1	1	1	1	1	1	1	1	1	1
1/2 F.S.	0	1	0	0	0	0	0	0	0	0	0	0
0 V + 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1
0 V	0	0	0	0	0	0	0	0	0	0	0	0
0 V - 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1
1/2 (-F.S.)	1	1	0	0	0	0	0	0	0	0	0	0
-F.S. + 1 LSB	1	0	0	0	0	0	0	0	0	0	0	1
-F.S.	1	0	0	0	0	0	0	0	0	0	0	0

Table for 12-bit D/A output or A/D input in ±5 V or ± 10 V ranges

NOTES:

(1) F.S. is full scale.
For -5V to +5 V range: F.S. = +5 V and -F.S. = 5 V.
For -10 V to +10 V range: F.S. = +10 V and -F.S. = -10 V.

(2) MSB is most significant bit. LSB is least significant bit. (See Table B-6 for voltage values per bit position.

Table B-5 12-Bit, Bipolar (+5 V, ± 10 V) Analog D/A or A/D)

	±5 V	±10 V	0 V to +10 V
MSB	Logic "1" Selects + Logic "0" Selects -	Logic "1" Selects + Logic "0" Selects -	.5
MSB-1	2.5	5.	2.5
-2	1.25	2.5	1.25
-3	.625	1.25	.625
-4	.3125	.625	.3125
-5	.15625	.3125	.15625
-6	.078125	.15625	.078125
-7	.0390625	.078125	.0390625
-8	.01953125	.0390625	.01953125
-9	.009765625	.01953125	.009765625
-10	.0048828125	.009765625	.0048828125
LSB	.00244140625	.0048828125	.00244140625

Table B-6 Voltage Values/Bit Positions for 12-Bit Analog Ranges

SAMPLE RANGE POINTS	CODE FOR RANGE POINTS									
	MSB	MSB -1	MSB -2	MSB -3	MSB -4	MSB -5	MSB -6	MSB -7	MSB -8	LSB
F.S. -1 LSB	1	1	1	1	1	1	1	1	1	1
+3/4 F.S.	1	1	0	0	0	0	0	0	0	0
+1/2 F.S.	1	0	0	0	0	0	0	0	0	0
+1/4 F.S.	0	1	0	0	0	0	0	0	0	0
0 V (or mA) +1 LSB	0	0	0	0	0	0	0	0	0	1
0 V (or mA)	0	0	0	0	0	0	0	0	0	0

Table for 10-bit D/A output in the 0 V to 10 V voltage range or the following current ranges: 0 - 20 mA and 0 - 5 mA

NOTES:

(1) F.S. is full scale. Full count (all "ones") yields F.S. -1 LSB.

(2) MSB is most significant bit. LSB is least significant bit. (See Table B-9 for voltage values per bit position. See Table B-10 for current values per bit position.)

Table B-7 10-Bit Resolution, Unipolar (0 V to 10 V) D/A Voltage Output

SAMPLE RANGE POINTS	CODE FOR RANGE POINTS									
	MSB	MSB -1	MSB -2	MSB -3	MSB -4	MSB -5	MSB -6	MSB -7	MSB -8	LSB
F.S. - 1 LSB	1	1	1	1	1	1	1	1	1	1
+3/4 F.S.	1	1	0	0	0	0	0	0	0	0
+1/2 F.S.	1	0	0	0	0	0	0	0	0	0
+1/4 F.S.	0	1	0	0	0	0	0	0	0	0
Offset + 1 LSB	0	0	0	0	0	0	0	0	0	1
Offset Value	0	0	0	0	0	0	0	0	0	0

Table for 10-bit D/A output in 1-5 mA and 4-20 mA ranges

Offset Values:

For 1-5 mA = 1.0 mA
For 4-20 mA = 4.0 mA

NOTES:

(1) F.S. is full scale. Full count (all "ones") yields F.S. -1 LSB. Zero count (all zeros yields the offset value (1.0 mA or 4.0 mA).

(2) LSB is least significant bit. MSB is most significant bit. (See Table B-10 for current values per bit position.)

Table B-8 10-Bit Resolution, Unipolar D/A Current Outputs

	±5 V	±10 V	0 V to 10 V
MSB	Logic "1" Selects + Logic "0" Selects -	Logic "1" Selects + Logic "0" Selects -	5.
MSB-1	2.5	5.	2.5
-2	1.25	2.5	1.25
-3	.625	1.25	.625
-4	.3125	.625	.3125
-5	.15625	.3125	.15625
-6	.078125	.15625	.078125
-7	.0390625	.078125	.0390625
-8	.01953125	.0390625	.01953125
LSB	.009765625	.01953125	.009765625

Table B-9 Voltage Values/Bit Position for 10-Bit Analog Ranges

	0 - 5 mA	0 - 20 mA	1 - 5 mA	4 - 20 mA
MSB	2.5 mA	10. mA	2. mA	8. mA
MSB-1	1.25	5.	1.	4.
-2	.625	2.5	.5	2.
-3	.3125	1.25	.25	1.
-4	.15625	.625	.125	.5
-5	.078125	.3125	.0625	.25
-6	.0390625	.15625	0.03125	.125
-7	.01953125	.078125	0.015625	0.0625
-8	.009765625	.0390625	0.0078125	0.03125
LSB	.0048828125	.01953125	0.00390625	0.015625

These values are referenced to the offset bias. (E.g., if the MSB is set in the 1-5 mA range, the resultant current output is 2.0 mA + 1.0 mA offset, or 3.0 mA. If the LSB were set in the 1-5 mA range, the resultant output would be 1.00390625 mA. If all zeros were used in the count for the 1-5 mA range, the output would be the offset value, 1.0 mA.)

Table B-10 Current Values/Bit Position in 10-Bit 0 to 5, 0 to 20, 1 to 5, and 4 to 20 mA Ranges

TDC 4500 COMPUTER SYSTEM INSTRUCTIONS

General Information: Instructions used by the 4500 Computer system are described briefly in this appendix. Some may not be recognized by PAL assemblers. Refer to the TDC 4500 Programming Manual for more details and other considerations..

The format of the 24-bit instruction word is illustrated with the description of each instruction. Execution times given are non-indexed and approximate. Indexing adds to the execution time listed. Various symbols are used in the descriptions, which are defined as follows:

A - A Register

C - Contents of

F/F - Flip-flop

J - J Counter

K - A constant, in some cases an address constant

P - P Register

Q - Q Register (main memory location 10_8)

X - Index Register (main memory locations 1-7). In format illustrations, X indicates that the instruction may be index modified.

Y - Operand address portion of an instruction.

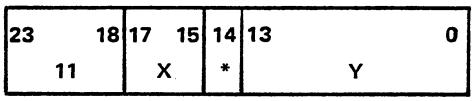
Z - The effective operand address resulting from index modification and relative address modification.

* - Relative address modification takes place if bit 14 is set.

Instructions with four character symbols are not recognized by standard assemblers.

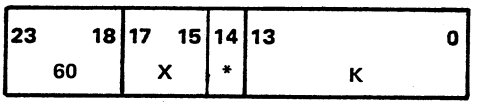
Full Operand Instructions

ADD - Add A to Z. ADD sums the contents of memory location Z with the contents of the A Register. If the result is too large to be stored in the 23 data bits of the A Register, the overflow flip-flop is set.



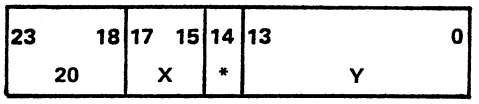
Z = f(X,*,Y)

AKA - Add K to A. AKA adds Z to the contents of the A Register. Any carry out of bit A_{23} will set the overflow flip-flop and be lost.



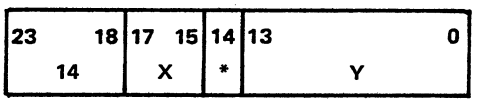
Z = f(X,*,K)

ANA - Logical AND to A. ANA performs the logic AND of the contents of memory cell Z with the contents of A. The corresponding bits of Z and A are compared. If the corresponding bits are both "one", a "one" is placed in that position of A. If either or both of the compared positions are "zero", a "zero" is placed in that position of A.



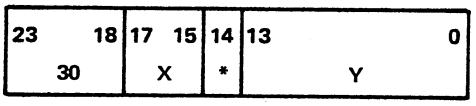
Z = f(X,*,Y)

BRU - Branch Unconditionally. BRU unconditionally transfers program control to the designated memory address Z. This is accomplished by calculating the address Z, if it is relative addressed and/or indexed, and then transferring this address to the Program (P) Register.



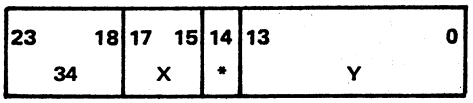
Z = f(X,*,Y)

BTR - Branch if Test Flip-Flop Reset. BTR transfers program control to memory location Z if the test flip-flop is reset. If the test flip-flop is set, program control continues in sequence (i.e., C (P) + 1). The status of the test flip-flop is not changed by the BTR command.



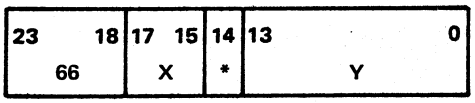
Z = f(X,*,Y)

BTS - Branch if Test Flip-Flop Set. BTS transfers program control to memory location Z if the test flip-flop is set. If the test flip-flop is reset, program control continues in sequence (i.e., C (P) + 1). The status of the test flip-flop is not changed by the BTS command.



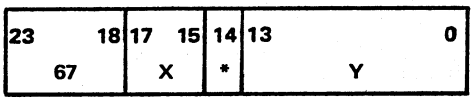
Z = f(X,*,Y)

CME - Compare Memory Equal. Compare memory equal compares the value of the operand Z with the contents of the A Register. If the two values are not equal, the test flip-flop is reset. No other indicators are affected.



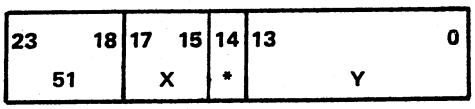
Z = f(X,*,Y)

CML - Compare Memory Less. Compare memory less compares the value of memory location Z with the contents of the A Register. If the A Register value is numerically less than memory location Z, the test flip-flop is set. If the operand value is greater than or equal to the value of the accumulator, the test flip-flop is reset. No other indicators are affected.



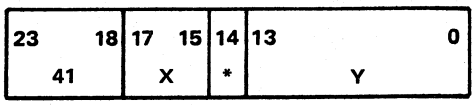
Z = f(X,*,Y)

DAD - Double Add. DAD places the sum of the double length numbers (A, Q) and (Z, Z + 1) into A_{23-0} and Q_{22-0}. Bit 23 in both Q and Z + 1 must be zero before execution. After executing the DAD, A_{23-0} contains the sign and most significant half of the sum. Q_{22-0} contains the least significant half of the sum. Q_{23} is reset to 0.



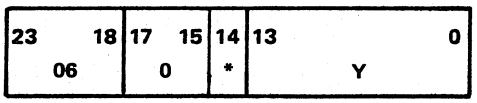
Z = f(X,*,Y)

DLD - Double Load. DLD places the contents of memory locations Z and Z + 1 into the A and Q Registers respectively.



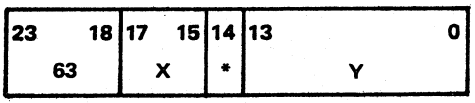
Z = f(X,*,Y)

DMT - Decrement Memory and Test. DMT subtracts 1 from the contents of memory cell Z each time it is executed. If the DMT is not the result of an API and the original contents of Z were not equal to 0, the test flip-flop is set. If the original contents of Z were equal to 0 and the DMT command is not the result of an API, the test flip-flop is cleared. If the DMT command is the result of an API and the original contents of Z were equal to 0, a signal is applied to API for ECHO generation. The test flip-flop is not affected by a DMT resulting from an API. DMT may not be indexed.



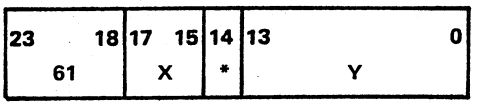
Z = f(Y,*)

DST - Double Store. DST places the contents of the A and Q Registers into memory locations Z and Z + 1 respectively.



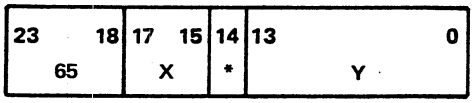
Z =f(X,*,Y)

DSU - Double Subtract. DSU subtracts the double length numbers (Z, Z + 1) from (A, Q) and places the result in A_{23-0} and Q_{22-0}. Bit 23 must be set in both Q and Z + 1 before the instruction is executed. During execution Q_{23} will be reset to 0. The overflow flip-flop is set if arithmetic overflow occurs.



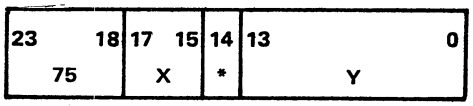
Z = f(X,*,Y)

DVD - Divide. DVD divides the 47-bit dividend, 24 bits of the A Register coupled with bits 22 through 0 of the Q Register, by the divisor contained in location Z. The quotient is placed in the Q Register and the remainder is placed in the A Register. If the quotient is too large to be contained in the Q Register, the overflow flip-flop is set. The sign of A (A_{23}) applies to the remainder, and the sign of Q (Q_{23}) applies to the quotient.



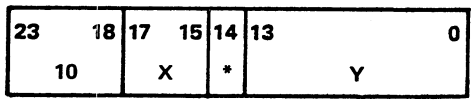
Z = f(X,*,Y)

DVM - Divide Magnitude. DVM divides A_{23-0} coupled with Q_{22-0} by the divisor from location Z. DVM places the quotient in the Q Register and the remainder in the A Register. The sign of the remainder will be the same as the sign of the dividend.



Z = f(X,*,Y)

ERA - Exclusive OR to A. ERA compares the corresponding bits of A with those of memory cell Z. If the corresponding bits of both A and Z are alike, a "zero" is placed in that position of A. If the corresponding bits of A and Z are not alike, a "one" is placed in that position of A.

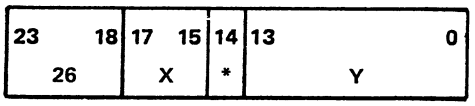


Z = f(X,*,Y)

INX - Increment X. INX adds the numeric value of Z to the contents of the X location cell specified by bits 17 through 15 of the command. The value of K must have a value within the range of +8,191 to -8,192.

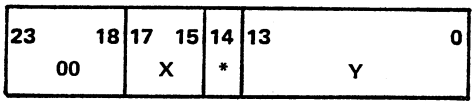
NOTE

An INX command specifying to increment X cell 2 by zero (26200000) is NOP - No Operation. If the index field of the INX command (17 through 15) is equal to zero, the instruction is undefined.



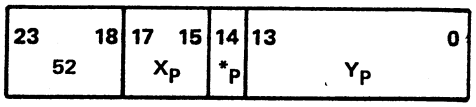
Z = f(K,*)

LDA - Load the A Register. LDA places the contents of memory location Z into the A Register. The contents of memory location Z are unchanged.



Z = f(X,*,Y)

LDI - Load Indirect. LDI loads the A Register with the contents of the memory location whose absolute address is W. The value of W may range from 0 to 262,144. W is defined in memory location Z.

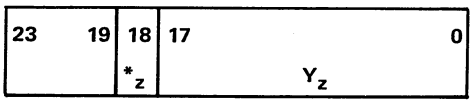


Z = f(X_P,$*_P$,Y_P)

If bit 18 is set in memory location Z, then $W = Y_Z + Z$.

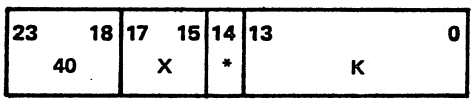
If bit 18 is not set in memory location Z, then $W = Y_Z$.

Memory location Z has the following format:



W = f(Y_Z,$*_Z$)

LDK - Load A with K. LDK places the positive value Z right justified into the A Register. The A Register is cleared prior to loading with Z. The value of K may be as large as 16383.

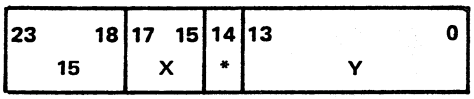


Z = f(X,*,K)

List Instructions - The List instructions are described briefly in part 4.1.8 of this General Description. They are:

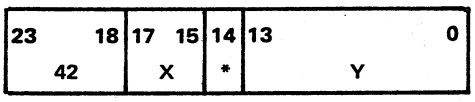
Op-Code	Instruction
47X*Y	AEL Append Item to End of List
57X*Y	ABL Append Item to Beginning of List
46X*Y	REL Remove Item from End of List
56X*Y	RBL Remove Item from Beginning of List

LDP - Load Place. LDP transfers program control to the location specified by the contents of Z_{17-0}. The permit automatic interrupt flip-flop is loaded from bit 21 of Z. On the 4500B, the trapping mode flip-flop is set if bit 19 of Z is set. This instruction is similar to an LPR, except the overflow, floating point mode and test flip-flops are not restored.



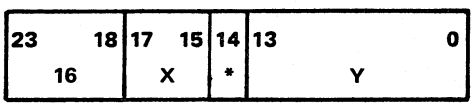
Z = f(X,*,Y)

LDQ - Load the Q Register. LDQ places the contents of memory location Z into the Q Register (memory location 10_8). The contents of memory location Z are unchanged by the LDQ command.



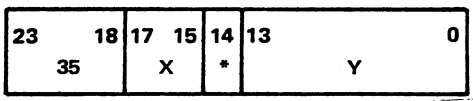
Z = f(X,*,Y)

LDX - Load X Location from Z. LDX places the contents of memory location Z into the specified (bits 17 through 15) index register. If the index field (bits 17 through 15) of the LDX command are zero, the command is undefined.



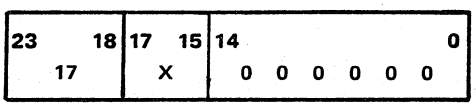
Z = f(Y,*)

LPR - Load Place and Restore. LPR restores the status of the floating point precision, overflow flip-flop, permit automatic interrupt flip-flop, and test flip-flop from the contents of bits 23-20, respectively, in memory location Z. LPR transfers program control to the location specified by the contents of Z17-0. If bit 19 of Z is a "one", the trapping mode flip-flop is set. If bit 19 of Z is a "zero", the status of the trapping mode flip-flop is unchanged.

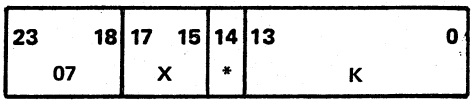


Z = f(X,*,Y)

LXC - Load X with Count. LXC 'ORs' the contents of the J counter into the specified X Register. On the 4500B, only the lower 5 J counter bits are 'ORed' into the X Register.

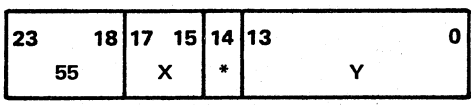


LXK - Load X with K. LXK stores the value Z into the addressed X Register. Leading bits of the register are set to "zero". The range of K, when not relative addressed, may vary from 0 to +16,383. The range of K when relative addressed may vary from -8,192 to +8,191 since bit 13 represents the sign of bits 12-0 when relative addressed. If bits 17, 16, and 15 of the LXK command are zero, the command is undefined (i.e., an X Register must be specified).



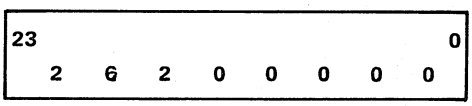
Z = f(K,*)

MPY - Multiply. MPY forms the product of the contents of memory cell Z (multiplicand) and the contents of the Q Register (multiplier). The contents of the A Register are added algebraically to the least significant half of the product. Thus, with proper scaling, it is possible to form the value C(Q)·C(Z) +A. This is stored in A_{23-0} and Q_{22-0}, with the most significant half in A. Bit 23 of Q is set to "zero" and is not a part of the product. The sign of A (A_{23}) applies to the entire product. Either positive or negative (2's complement) values may be multiplied, with the correct product, positive or negative (2's complement), contained in A and Q.

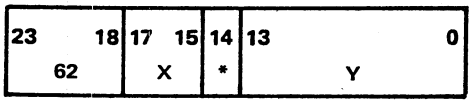


Z = f(X,*,Y)

NOP - No Operation. NOP transfers program control to the next sequential location (P + 1). No operation is performed.

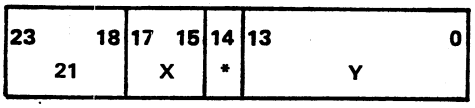


OOM - Operate on Memory. OOM specifies a memory location Z to function as the A Register for the next sequential instruction. The contents of Q are replaced with the contents of A. The contents of A are left unchanged. The Object instruction of the OOM is not interruptible and should not be a double length of Quasi instruction.



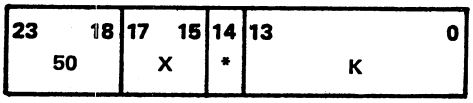
Z = f(X,*,Y)

ORA - Logical OR to A. ORA performs the logical OR of the contents of memory location Z with the contents of the A Register. Each bit of Z is compared with the corresponding bit of A. When either or both is a "one", a "one" is placed in that position of A. When both bits are "zero", that position of A is not changed.



Z = f(X,*,Y)

SKA - Subtract K from A. SKA subtracts (Z) from (A) and places the result into A.

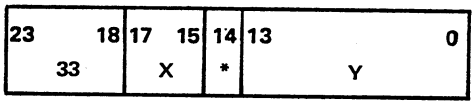


Z = f(X*K)

SPB - Save Place and Branch. SPB places the status of the floating point mode, overflow, permit automatic interrupt, test, trapping mode and IAI2 flip-flops in bit positions 23 through 18, respectively, of index register 1. The contents of the P Register, plus 1*, are stored in bits 17 through 0 of index register 1. The SPB command resets the floating point precision and permit automatic interrupt flip-flops, inhibiting level 2 (inhibitable) interrupts. The trapping mode flip-flop is cleared if the SPB command is executed as a result of an automatic program interrupt.

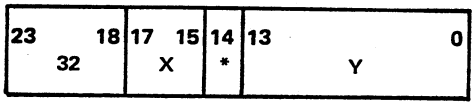
*** NOTE**

The address that is stored by the SPB command is normally the address of the SPB command plus 1. However, there are exceptions. If an SPB command is performed due to the use of XEC or Quasi commands, the address of the XEC or Quasi plus 1 is stored. If SPB is executed immediately following an acknowledged automatic program interrupt or memory protect trap. P contains the address of current program control. In these cases, the value saved in Index Register 1 is P, the first unexecuted instruction in the interrupted program (i.e., the address to which program control will return when the interrupt has been serviced).



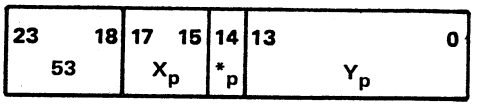
Z = f(X,*,Y)

STA - Store Contents of A. STA places the contents of the A Register into memory location Z. The contents of the A Register are unchanged.



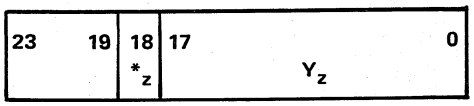
Z = f(X,*,Y)

STI - Store Indirect. STI places the contents of the A Register into the memory location whose absolute address is W. The range of W is from 0 to 262,144. W is defined by memory location Z.



$Z = f(X_p, *_p, Y_p)$

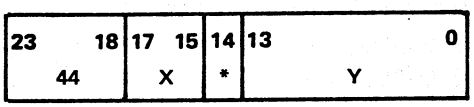
The format of location Z is:



$W = f(Y_p, *_z)$

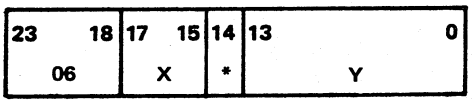
If bit 18 of (Z) = 0, then $W = Y_Z$. If bit 18 of (Z) = 1, then $W = Y_Z + Z$.

STQ - Store Contents of Q. STQ places the contents of the Q Register (memory location 10_8) into memory location Z. The contents of the Q Register are unchanged by the STQ command.



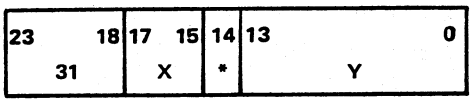
Z = f(X,*,Y)

STX - Store X Location into Z. STX stores the contents of the indicated X Register into memory location Z. The Z address may not be indexed as bits 15, 16, and 17 are used to specify the X Register to be stored. If no index address is indicated, the STX command is executed as a DMT command.



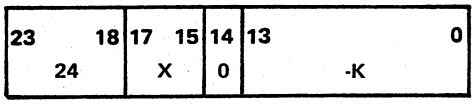
Z = f(Y,*)

SUB - Subtract Z from A. SUB performs algebraic subtraction of the contents of memory location Z from the contents of the A Register. The result of the subtraction is stored in the A Register. If the result is too large to be stored in the 23 bits of A (i.e., more negative than -2^{23} or more positive than $2^{23}-1$), the overflow flip-flop is set.

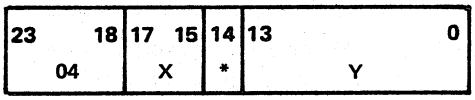


Z = f(X,*,Y)

TXH - Test X High or Equal. TXH sets the test flip-flop if the contents of the specified X cell (bits 17-0) are greater than or equal to the value K. If the contents of X_{17-0} are less than K, the test flip-flop is cleared. Bits 15, 16, and 17 of the TXH command specify the address of the X cell to be compared. The K value of the TXH command must be specified in 2's complement form. The value of the index cell contents may vary between 0 and 262,143. The value of K may range between 16,383 and 1. The contents of the addressed X cell are not changed by the TXH command. If bits 15, 16, and 17 are "zero", the command is undefined, i.e., an X cell address must be specified.



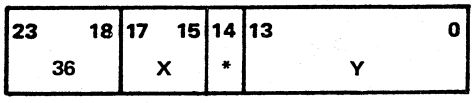
XEC - Execute. XEC indicates the address Z of the next instruction to be executed. Program control does not change, that is, the P Register is not incremented and the program continues in sequence after executing the instruction located at the effective operand address. All instructions including XEC, may be executed. If the Object instruction (contents of cell Z) is relative addressed, the effective operand of the Object instruction is computed from the location of the Object instruction rather than from the contents of the P Register.



Z = f(X,*,Y)

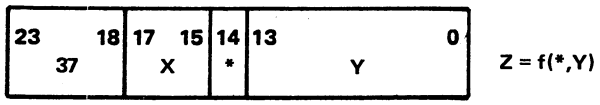
Field Instructions - The Field instructions move 1 to 24 adjacent bits between memory and the A Register. Each Field instruction refers to a "descriptor" word in memory to determine which bits should be moved and to or from what memory location. The descriptor word is described later.

LDF - Load Field. Load Field replaces the least significant bits of the A Register with those from the memory location specified by the descriptor word Z. If the sign extension bit in the descriptor word is 0, the most significant A Register bits are cleared. If the sign extension bit is equal to 1 then the most significant bit of the field is loaded into the upper A Register bits.

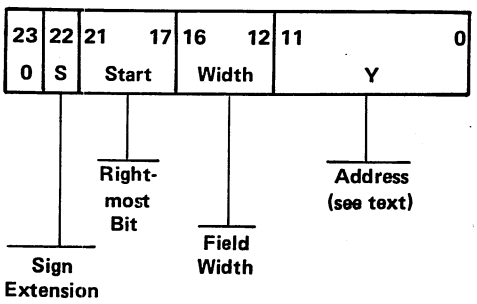


Z = f(*,Y)

STF - Store Field - Store Field stores the least significant A Register bits into the field of a memory location specified by the descriptor word Z. The sign extension bit has no use in this instruction and the contents of the A Register is not changed.



Descriptor Word - The operand of the LDF or STF command points to a memory location Z to specify field width and other details. When bit 23 of the descriptor word is equal to 0, then bits 22-0 describe the field operation as follows:



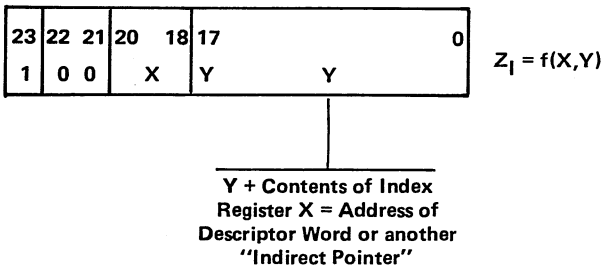
- The start bit may be any value between 0 and 23_{10}.
- The width must be a value between 1 and 24_{10}.

> **NOTE**
>
> The sum of the start and width field must not exceed 24 (i.e., the field must be wholly contained in one memory word).

- Address (Y) - If the STF/LDF is not indexed, then Y is the memory address (locations 0-2047_{10}) from/to which the field of data will move.

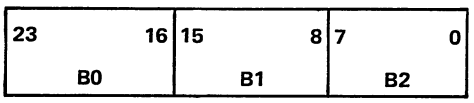
  If the STF/LDF is indexed, the Y field plus the contents of index register X are added to find the effective memory address to/from which the data field will move.

If bit 23 is set in the memory location Z specified by an LDF or STF operand, then the location Z contains an "indirect pointer" to the descriptor word or to another indirect pointer word and has this format:



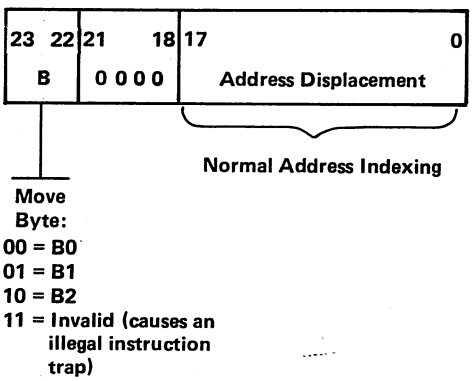
Use of an indirect pointer adds 3 μs to the execution time.

Byte Handling Instructions - Byte instructions move 8-bit bytes of data between memory and the A Register. Each data word is treated as a group of three bytes like this:

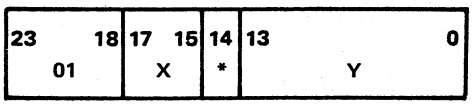


Byte instructions use bits 17-15 to specify an Index Register. Like any full operand indexing operation, bits 0-17 of the Index Register are added to the instruction operand field to form the address of the data in memory. Byte instructions use bits 23 and 22 to specify which byte of the memory word will be loaded or stored.

The Index Register format is:



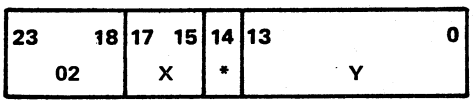
LBY - Load Byte loads A Register bits 0-7 with a byte from memory location Z. A Register bits 8-23 are cleared. The byte (B0, B1, or B2) is specified by bits 23 and 22 of the Index Register.



Z = f(X,*,Y)

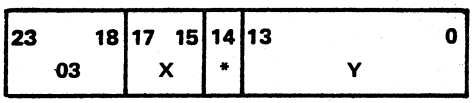
Incrementing Byte Instructions - With each execution, these instructions update the Index Register B field to select the next byte. After byte B2, one is added to the address displacement field and bits 22-23 are cleared to select B0 from the next memory location.

LBI - Load Byte and Increment loads A Register bits 0-7 with a byte from memory (same as LBY). Bits 8-23 of the A Register are cleared. The Index Register is then incremented to point to the next byte as explained above.



Z = f(X,*,Y)

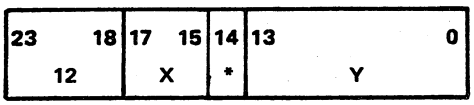
SBI - Store Byte and Increment stores bits 0-7 of the A Register into memory location Z. The byte position (B0, B1, or B2) is specified by bits 22 and 23 of the Index Register. Bit 21 of X must be zero. Contents of the other two bytes are unchanged. The Index Register is then incremented to point to the next byte.



Z = f(X,*,Y)

Sometimes it is desirable to skip forward or backward in memory to a new group of bytes. This can be done with the ABP command.

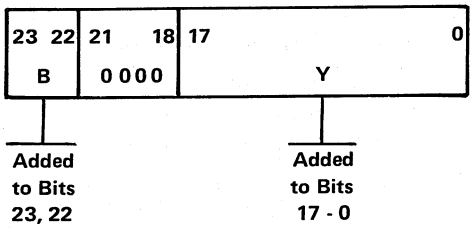
ABP - Adjust Byte Pointer is used to add or subtract bits 23, 22, and 0-17 of memory location Z to the Index Register specified in bits 17-15 of the ABP instruction.



Z = f(*,Y)

Memory location Z:

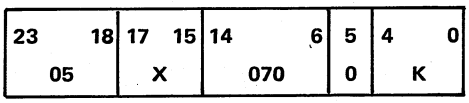
must have bits 18-21 = 0
must not have bits 22, 23 = 11.



The hardware will automatically use base three arithmetic when adding bits 22 and 23 to (X). Carries are added to bits 0-17 of the Index Register.

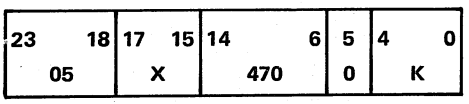
GEN 1 Instructions

ADO - Add One to Bit K. ADO adds plus one to bit position Z in the A Register. Carries out of A_{23}, resulting from the summation, are lost, but the overflow flip-flop is not affected.



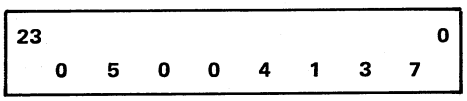
Z = f(X,K)

CBK - Change Bit K. CBK complements bit Z of the A Register. All other bit positions of A remain unchanged. If Z exceeds 23 (decimal), A will be unchanged.

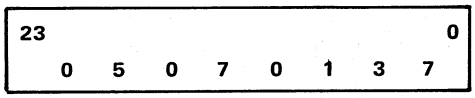


Z = f(X,K)

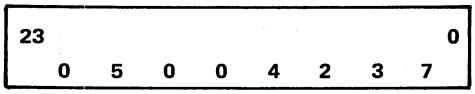
CLO - Count Least Significant Ones. CLO counts the number of "one" bits to the right of the rightmost "zero" bit in the A Register. The count value is placed in the J counter. If A equals 77777777_8, the count in J is 24_{10}.



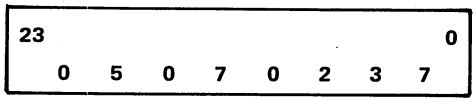
CLZ - Count Least Significant Zeros. CLZ counts the number of "zero" bits to the right of the rightmost "one" bit in the A Register. The count value is placed in the J counter. If A equals 00000000_8, the count in J is 24_{10}.



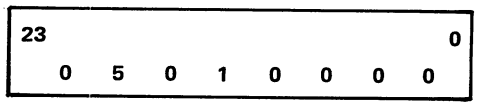
CMO - Count Most Significant Ones. CMO counts the number of "one" bits to the left of the leftmost "zero" bit in the A Register. The count value is placed in the J counter. If A equals 77777777_8, the count in J is 24_{10}.



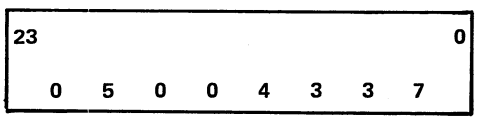
CMZ - Count Most Significant Zeros. CMZ counts the number of "zero" bits to the left of the leftmost "one" bit in the A Register. The count value is placed in the J counter. If A equals 00000000_8, the count in J is 24_{10}.



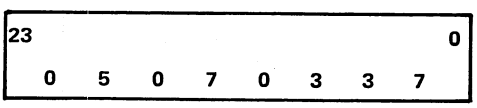
CPL - Complement A. CPL inverts each bit in the A Register; that is, each "one" is replaced by a "zero" and each "zero" is replaced by a "one".



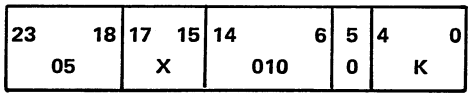
CTO - Count Total Ones. CTO counts the total number or "one" bits in the A Register. The count value is placed in the J Counter. If A equals 77777777, the count in J is 24_{10}.



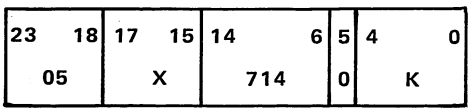
CTZ - Count Total Zeros. CTZ counts the total number or "zero" bits in the A Register and the count value is placed in the J Counter. If A equals 00000000, the count in J is 24_{10}.



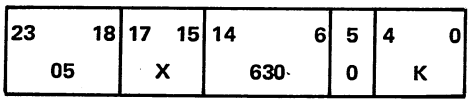
IBK - Isolate Bit K. IBK leaves bit Z of the A Register unchanged and clears all other bits in A.*



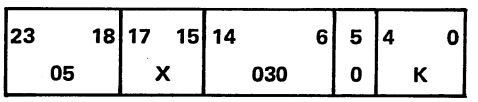
ICB - Isolate and Complement Bit K. ICB complements bit Z of the A Register. All other bits in A are cleared. If Z is greater than 23, all A Register bits are cleared.



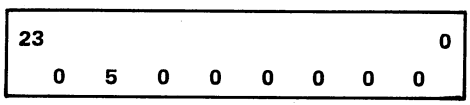
LBM - Load Bit Mask. LBM places "zero" in bit Z of the A Register and sets all other bits in A to "one".*



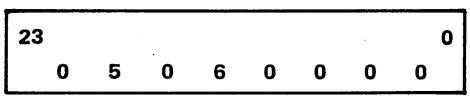
LDO - Load One into Bit K. LDO places a "one" in bit Z of the A Register. All other bits of A are cleared (zero).*



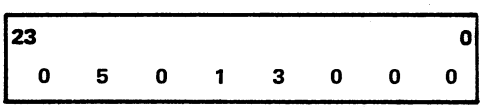
LDZ - Load Zeros into A. LDZ replaces the contents of the A Register with "zeros".



LMO - Load Minus One into A. LMO places a "one" in each bit of the A Register (equals minus 1).

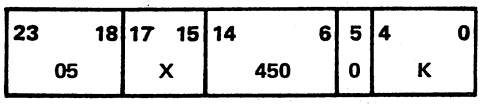


NEG - Negate. NEG replaces the contents of the A Register with its 2's complement value.

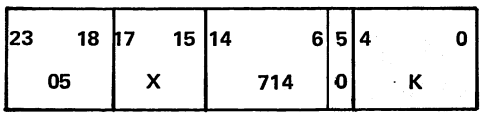


*For Z greater than 23 (decimal), A will be set to zeros.

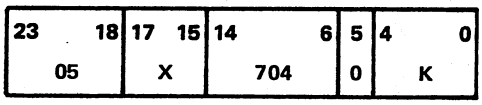
RBK - Reset Bit K. RBK places a "zero" into bit Z of the A Register. All other bits in A remain unchanged.



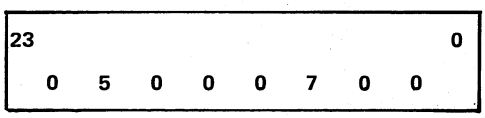
RER - Reset Test Flip Flop if bit K is even and Reset bit K. RER clears the Test Flip Flop if A Register bit Z is a "zero". Bit Z is cleared if it is a "one" but the Test Flip Flop is unchnaged.



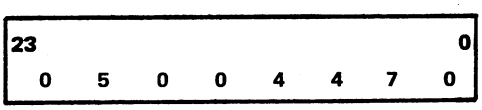
REV - Reset Test Flip-Flop if Bit K is Even. REV clears the test flip-flop if bit Z in the A Register is a "zero". If bit Z is a "one", the status of the test flip-flop is unchanged.



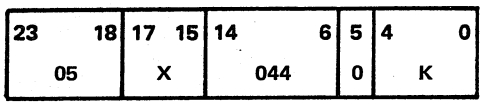
RLZ - Reset the Test Flip Flop and Load Zeros into A.



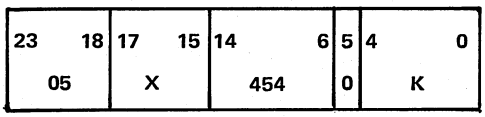
RNZ - Reset Test Flip-Flop if A is Non-Zero. RNZ clears the test flip-flop if any bit in the A Register is a "one". If all bits in A are "zero", the status of the test flip-flop is unchanged. The original contents of A are unchanged by the RNZ command.



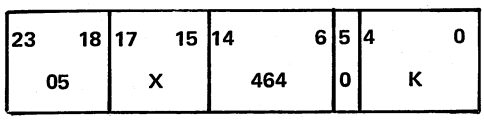
ROD - Reset Test Flip-Flop if Bit K is Odd. ROD clears the test flip-flop if bit Z in the A Register is a "one". If bit Z is a "zero", the status of the test flip-flop is unchanged. The original contents of A are unchanged by the ROD command.



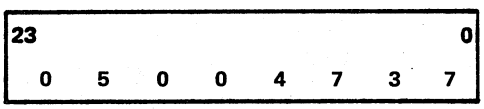
ROR - Reset Test Flip Flop if bit K is Odd and Reset bit K. If A Register bit Z is a "one", ROR resets the Test Flip Flop and resets bit Z. If A Register bit Z is a "zero", ROR does not affect the Test Flip Flop or bit Z.



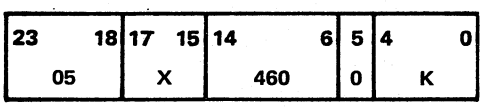
ROS - Reset the Test Flip Flop if bit K is Odd and Set bit K. If A Register bit Z is "one", ROS resets the Test Flip Flop. If A Register bit Z is a "zero", the Test Flip Flop is unchanged and bit Z is set to a "one".



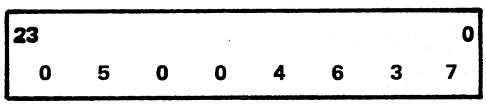
RST - Reset the Test Flip-Flop. RST unconditionally clears the test flip-flop. The contents of A are unchanged by RST.



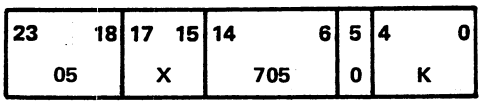
SBK - Set Bit K. SBK sets bit Z in the A Register to "one". All other bits in the A Register are unchanged.



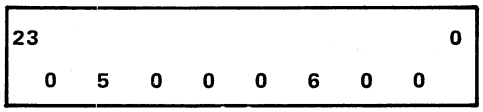
SET - Set Test Flip-Flop. SET unconditionally sets the test flip-flop. The original contents of the A Register are unchanged.



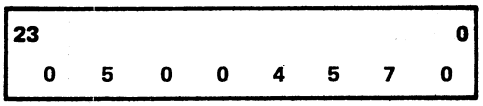
SEV - Set Test Flip-Flop if Bit K is Even. SEV sets the test flip-flop if bit Z in the A Register is a "zero". If bit Z in A is a "one", the status of the test flip-flop is unchanged.



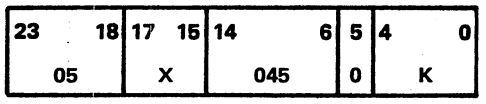
SLZ - Set the Test Flip Flop and load "Zeros" into the A Register.



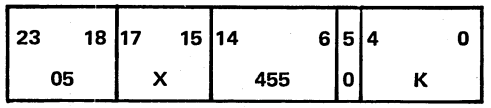
SNZ - Set Test Flip-Flop if A is Non-Zero. SNZ sets the test flip-flop if any bit in the A Register is a "one". If all bits in A are "zero", the status of the test flip-flop is unchanged.



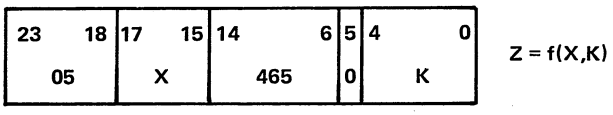
SOD - Set Test Flip-Flop if Bit K is Odd. SOD sets the test flip-flop if bit Z in the A Register is a "one". If bit Z in A is a "zero", the status of the test flip-flop is unchanged.



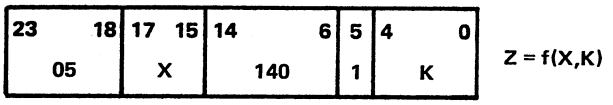
SOR - Set Test Flip Flop if bit K is Odd and Reset bit K. If A Register bit Z is a "one", SOR sets the Test Flip Flop and resets bit Z. If A Register bit Z is a "zero", the Test Flip Flop and bit Z are unchanged.



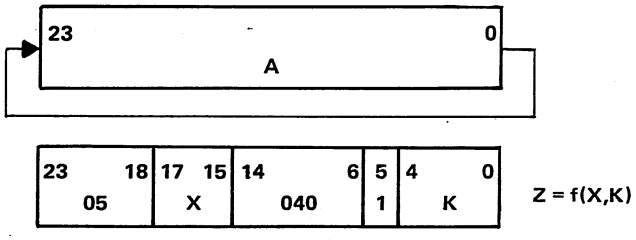
SOS - Set the Test Flip Flop if bit K is Odd and Set bit K. If A Register bit Z is a "one", the Test Flip Flop is set. If bit Z is a "zero", the Test Flip Flop is unchanged but bit Z is set to a "one".



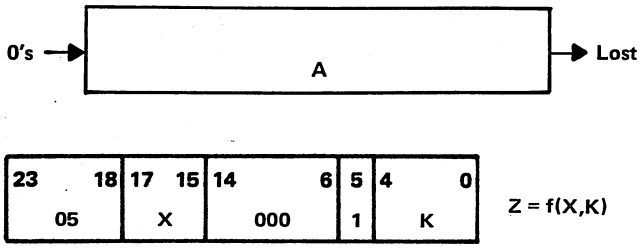
SRA - Shift A Right Arithmetic. SRA shifts the contents of the A Register Z places to the right. The sign bit (23) of A is unchanged. Bits shifted out of A_0 are lost. Bits shifted into A_{22} are the same as the sign bit. The maximum number of shifts is 24 places.



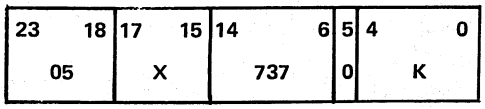
SRC - Shift Right Circular. SRC shifts the contents of the A Register Z places to the right in a circular fashion; that is, the bit shifted from A_0 is inserted in A_{23}, replacing the bit shifted out of A_{23}. The maximum number of shifts is 24.



SRL - Shift Right Logical. SRL shifts all 24 bits of the A Register to the right Z places. Zeros are shifted in through A_{23}. Bits shifted out of A_0 are lost. The maximum number of shifts is 24 places.

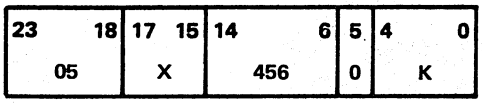


TEC - Test bit K for Even and Complement bit. TEC sets the Test Flip Flop if A Register bit Z is a "zero", and bit Z is then changed to a "one". If bit Z is a "one", TEC changes it to a "zero" and the Test Flip Flop is unchanged.



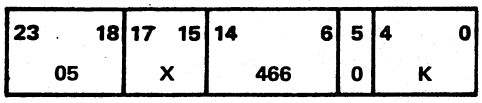
Z = f(X,K)

TER - Test Even and Reset Bit K. TER sets the test flip-flop if bit Z in the A Register is "zero", and places a "zero" back in bit Z. If bit Z is "one", the test flip-flop is cleared and a "zero" is placed in bit Z.



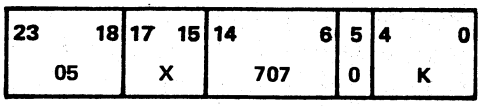
Z = f(X,K)

TES - Test Even and Set Bit K. TES sets the test flip-flop if bit Z in the A Register is a "zero", and replaces bit Z with a "one". If bit Z is a "one" the test flip-flop is cleared and a "one" is placed back in bit Z.



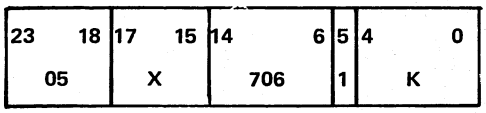
Z = f(X,K)

TEV - Test Bit K Even. TEV sets the test flip-flop if bit Z in the A Register is "zero". If bit Z in the A is "one", the test flip-flop is cleared.



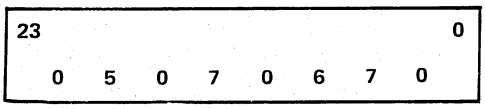
Z = f(X,K)

TMF - Test K bits for Minus one. TMF sets the Test Flip Flop if all of the lower Z bit positions in the A Register are "ones". If any of the lower Z bit positions in the A Register is a "zero", the Test Flip Flop is unchanged.

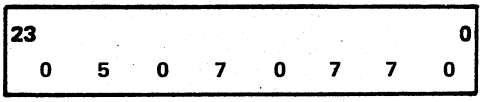


Z = f(X,K)

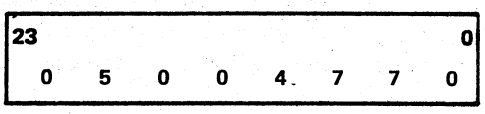
TMO - Test A for Minus One. TMO sets the Test Flip Flop if all A Register bits are "ones". If any A Register bit is a "zero", the Test Flip Flop is unchanged.



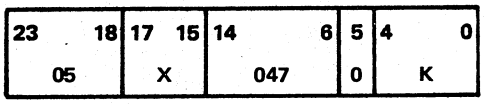
TNM - Test Not Minus One. TNM sets the test flip-flop if any bit in the A Register is a "zero". When all bits of the A Register are "ones" (minus 1) the test flip-flop is cleared.



TNZ - Test A Non-Zero. TNZ sets the test flip-flop if any bit in the A Register is a "one". If all bits in the A Register are "zero", the test flip-flop is cleared.

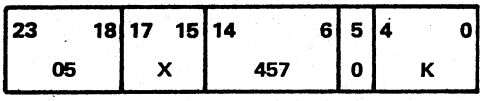


TOD - Test Bit K Odd. TOD sets the test flip-flop if bit Z in the A Register is a "one". If bit Z in A is "zero", the test flip-flop is cleared.



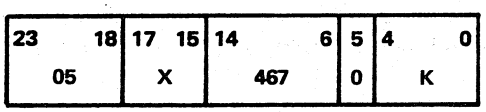
Z = f(X,K)

TOR - Test Odd and Reset Bit K. TOR sets the test flip-flop if bit Z in the A Register is a "one", and replaces bit Z with a "zero". If bit Z in A is a "zero", the test flip-flop is cleared and bit Z remains "zero".



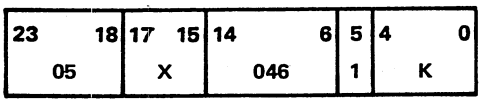
Z = f(X,K)

TOS - Test Odd and Set Bit K. TOS sets the test flip-flop if bit Z in the A Register is a "one" and bit Z remains a "one". If bit Z in A is a "zero", the test flip-flop is cleared and bit Z is replaced with a "one".

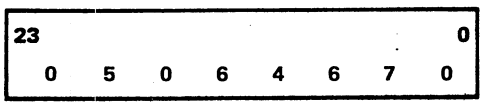


Z = f(X,K)

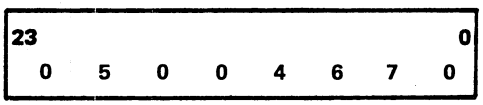
TSC - Test and Shift Circular. TSC shifts the contents of the A Register right circular Z places. If all bits shifted out of A_0 are "zero", the test flip-flop is set, otherwise it is cleared. The maximum number of shifts is 24_{10}.



TZC - Test Zero and Complement. TZC sets the test flip-flop if all bits in the A Register are "zero". If any bit in the A Register is a "one", the test flip-flop is cleared. TZC also replaces the contents of the A Register with its 1's complement.

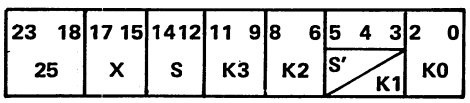


TZE - Test A Zero. TZE sets the test flip-flop if all bits in the A Register are "zero". If any bit in the A Register is a "one", the test flip-flop is cleared. The original contents of A are unchanged.



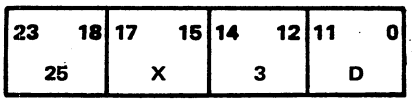
GEN 2 Instructions

All GEN 2 instructions have the following basic form.



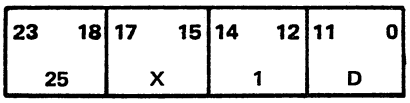
ABT - Abort Device D's Operation. ABT terminates the operation of the addressed device and initializes the addressed channel. The operation may or may not have been completed. Some device operations cannot be terminated instantly, therefore, the program must account for this delay. JNR detects completion of the operation.

S = 3, K3 ≠ 0



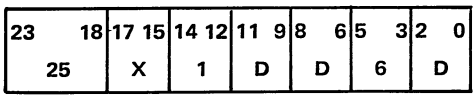
ACT - Activate Device D's Interrupt. ACT indirectly initiates programmed operation of device Z by initiating an automatic program interrupt from the device. If device Z is not in operation, ACT simulates the completion of an operation to provide the automatic program interrupt (i.e., the ready signal is cycled to not ready and back to ready). If device Z is in operation, the ACT command is ignored.

S = 1, K3 ≠ 0



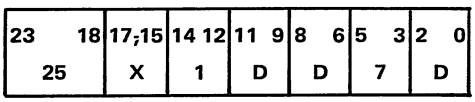
AIM* - Activate Interrupt Mask. AIM masks the interrupt pair from GENIE Bus device DDD, where DDD may range from 400_8 to 700_8. AIM may be executed at any time but it is good practice to mask and unmask interrupt pairs while all interrupts are inhibited by IAI2 so that the mask conditions are known when PAI is executed to permit servicing of interrupts.

S = 1, S' = 6



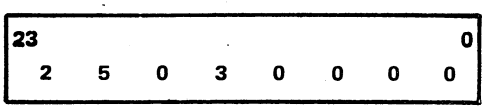
DIM* - Deactivate Interrupt Mask. DIM unmasks the interrupt pair from GENIE Bus device DDD, where DDD may range from 400_8 to 700_8. DIM may be executed at any time but it is good practice to mask and unmask interrupt pairs while all interrupts are inhibited by IAI2 so that the mask conditions are known when PAI is executed to permit servicing of interrupts.

S = 1, S' = 7



IAI - Inhibit Automatic Interrupt. IAI clears the permit automatic interrupt flip-flop to inhibit inhibitable program interrupts. Non-inhibitable interrupts are not affected by the IAI command or permit automatic interrupt flip-flop.

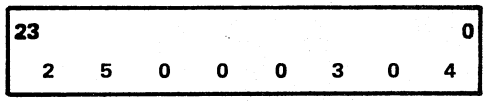
S = 3, K3 = 0



IAI2* (III) - Inhibit all Automatic Interrupts. IAI2 inhibits all interrupts, both inhibitable and non-inhibitable, provided the permit automatic interrupt flip-flop has been cleared previously.

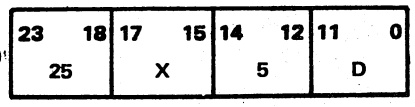
*These instructions are not recognized by all assemblers.

S = 4, K3 = 0



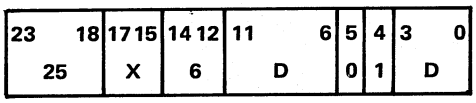
IN - Input from Device D. IN transfers data from the addressed device or channel to the A Register. The address, D, may specify any device or controller on the I/O Bus.

S = 5, K3 ≠ 0



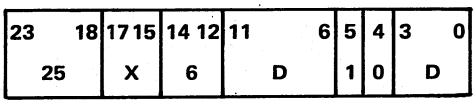
JCB - Jump if Channel Busy. JCB transfers program control to the second sequential instruction (P + 2) if busy. If the addressed channel is ready, program control is transferred to the first sequential instruction (P + 1).

S = 6, K3 ≠ 0



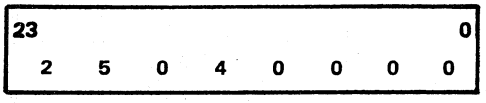
JDR - Jump if Data Ready. JDR transfers program control to the second sequential instruction (P + 2) if the addressed input channel is busy and its data ready indicator is set. Control is also transferred to the second sequential instruction (P + 2) when the addressed output channel is busy and its buffer ready indicator is set. If either indicator of the addressed channel is reset, program control is transferred to the first sequential location (P + 1). When the addressed channel is not busy, program control is transferred to the first sequential location (P + 1).

S = 6, K3 ≠ 0



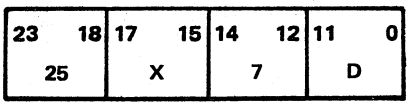
JND - Jump if No Demand. JND transfers program control to the second sequential location (P + 2) if the demand flip-flop is reset. If the demand flip-flop is set, JND clears it and advances program control to the first sequential location (P + 1). The demand flip-flop is set by pressing and then releasing the DEMAND switch on the computer console.

S = 4, K3 = 0



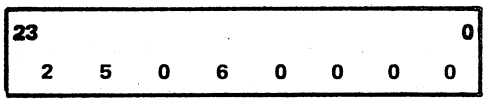
JNE - Jump if Device D Not in Error. JNE transfers program control to the second sequential location (P + 2) if no error or alarm exists in the addressed module. If an error or alarm exists, program control is transferred to the first sequential instruction (P + 1). Depending on the module addressed, the JNE command may also clear the error or alarm indicator in the module.

S = 7, K3 ≠ 0



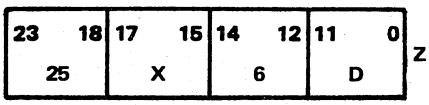
JNO - Jump if No Overflow. JNO transfers program control to the second sequential location (P + 2) if the overflow flip-flop is cleared. If the overflow flip-flop is set, JNO clears it and transfers program control to the first sequential location (P + 1).

S = 6, K3 = 0



JNR - Jump if Device D Not Ready. JNR transfers program control to the second sequential location (P + 2) if the addressed device (Z) is in operation. If the addressed device is "ready", JNR transfers program control to the first sequential location (P + 1).

S = 6, K3 ≠ 0



OPR - Operate. OPR is primarily used in conjunction with the peripherals on the I/O Bus. The specific function varies with each device. Typical uses are:

1. Initiate the I/O operation or addressed channel.
2. Transfer the contents of the A Register to the addressed channel.
3. Set the addressed channel to the busy state.

4. Clear the addressed channels Error/Alarm line.

S = 2, K3 ≠ 0

23 18	17 15	14 12	11 0
25	X	2	D

Z = f(X,D)

OUT - Output to Device D. OUT transfers data from the A Register to the addressed device. When the addressed device is a bulk memory controller, the contents of A are not used, but the OUT instruction initiates a bulk memory transfer. Except for bulk memory transfers, OUT performs two distinct functions: (1) specifies a device, and (2) transfers data to that device. This data may include control information.

S = 4, K3 ≠ 0

23 18	17 15	14 12	11 0
25	X	4	D

Z = f(X,D)

PAI - Permit Automatic Interrupt. PAI sets the permit automatic interrupt flip-flop and resets IAI2 to allow inhibitable program interrupts following the next interruptible command.

S = 2, K3 = 0

23							0
2	5	0	2	0	0	0	0

RCS - Read Console Switches. RCS places the contents of the console switch register into the A Register.

S = 5, K3 = 0

23							0
2	5	0	5	0	0	0	0

SEL - Select Device D. SEL enables a device (Z) in the input/output equipment, but performs no functional operation on, or with, the device. The SEL command is used only when timing requirements between the Arithmetic Unit and the device are such that the time allotted for an IN, OUT, ACT, etc., is not enough to complete a functional operation. IN, OUT, ACT, etc., contain selection and functional operation capabilities within the command, but where timing requirements between the AU and the I/O module are restrictive, the SEL command precedes these commands. The SEL command is not normally required for I/O modules currently in use.

S = 0, K3 ≠ 0

23 18	17 15	14 12	11 0
25	X	0	D

Z = f(X,D)

SSA - Set Stall Alarm (Optional). SSA resets a timer in the stall alarm circuitry. If the timer is allowed to "time out", because the program does not execute another SSA command to again reset the timer, an output signal is available to light the stall alarm and error indicators on the console and optionally halt computer sequencing, generate an interrupt, etc. Stall time is either 64, 128, or 256 power line cycles as selected by Jumper Clip option.

The stall alarm is used to detect a malfunction in the computer program or system that causes a hang-up or stall condition in program sequencing. The stall alarm circuitry is inhibited in the manual mode of operation or when the Stall Lockout switch is in the lockout position.

S = 1, K3 = 0

23							0
2	5	0	1	0	0	0	0

LPM - Load Protect Mode is used to set up the optional memory protect map. Refer to section 4 of this General Description for a detailed description of the A and Q Register formats used with this instruction.

S = 0, K3 = 0

23							0
2	5	0	0	0	4	0	0

Programmable Status - The programmable status GEN 2 commands provide the capability of enabling a relay driver, under program control, for optional use by the system. The relay driver is turned on by executing 25014000 and turned off by executing 25024000.

Alarm On SALM

23							0
2	5	0	1	4	0	0	0

Alarm Off
RALM

23							0
2	5	0	2	4	0	0	0

Control Bus Instructions - These instructions move information on the Memory/CPU Bus. This is normally done by the processor's firmware using its own special set of rules–which are beyond the scope of this publication. The user-level control bus instructions described below will be found in some Test and Diagnostic (T & D) programs and diagnostic areas of RTMOS.

There are two basic control bus operations: read and write.

CBR* - Control Bus Read. CBR performs a read operation from the device specified in the RID bits. The contents of the Q Register is used to further define the operation. Data returned by the responder device is placed in the A Register.

23 18	17 15	14 12	11 9	8 0
27	X	3	RID	000

CBW* - Control Bus Write. CBW performs a write operation to the device specified by the RID bits. The contents of the A Register is the data written. The contents of the Q Register is used to further define the desired operation.

23 18	17 15	14 12	11 9	8 0
27	X	3	RID	400

Responder Identification Codes - The RID codes used with these commands are:

0 Main Memory
1 Memory Bus Controller (MBC)
2 GENIE Bus Controller (GBC) - normal mode
3 GBC - interrupt mode
4 Reserved
5 Reserved
6 Reserved
7 Memory Protect Option

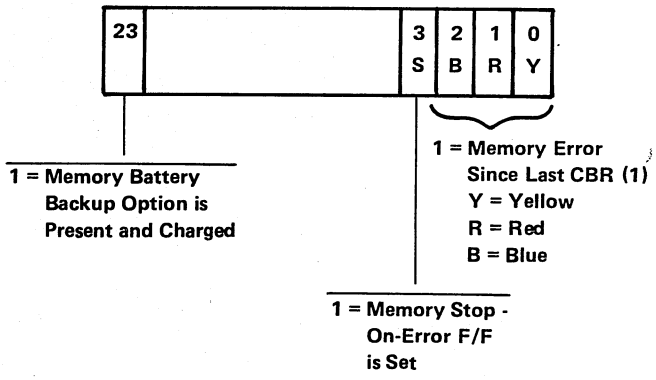
Some uses of the Control Bus instructions are:

( ) = RID

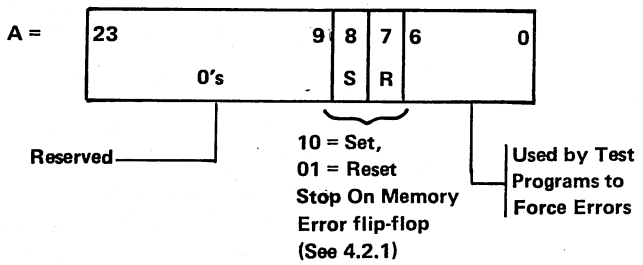
CBR (1) - Clear MBC yellow, red, blue errors, and read MBC status

*These instructions are not recognized by standard assemblers.

After a CBR1 the contents of A =



CBW (1) - Output to MBC



CBW (2) -

Q = 00074000 - Simulate System Reset

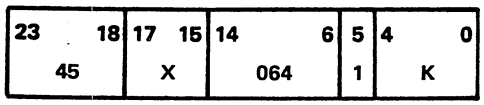
Resets the CPU and peripherals and brings the auto-reboot routine into memory.

Q = 00064000 - Simulate Power Fail

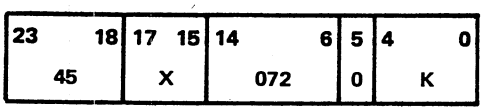
Cycles the power fail monitor circuitry. Resets the CPU and peripherals. Executes trap 22_8 if the Battery Backup option is present; otherwise it brings in the auto-reboot routine.

GEN 3 Instructions

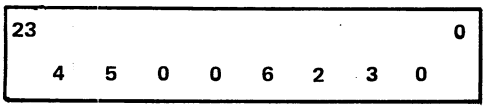
DLA - (Shift) Double Left Arithmetic. DLA shifts the contents of the A and Q Registers Z places to the left. Bits shifted out of Q_{22} enter A_0. Bits shifted out of A_{23} are lost. Bit Q_{23} is cleared. If any of the bits shifted into A_{23} are unlike A_{23}'s original contents, the overflow flip-flop is set. Zeros shift into Q_0.



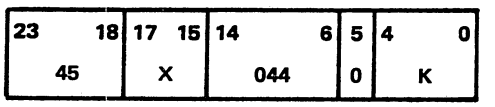
DLL - (Shift) Double Left Logical. DLL shifts the contents of the A and Q Registers Z places to the left. Bits shifted out of Q_{23} enter A_0. Bits shifted out of A_{23} are lost. Zeros shift into Q_0.



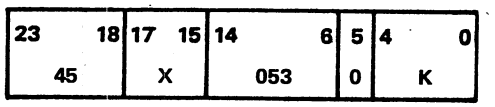
DLZ - Double Load Zeros. DLZ replaces the contents of the A and Q Registers with "zeros".



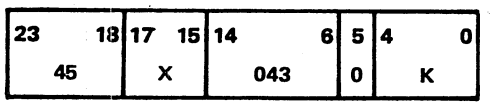
DRA - (Shift) Double Right Arithmetic. DRA shifts the A and Q Registers Z places to the right. Bits shifted out of A_0 are shifted into Q_{22}. Bits shifted out of Q_0 are lost. Bits shifted into A_{22} are the same as A_{23}. A_{23} remains unchanged and A_{23} is cleared. Bit Q_{23} is reset to 0.



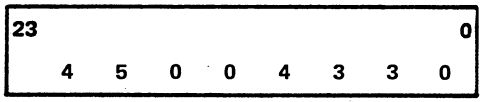
DRC - (Shift) Double Right Circular. DRC shifts all 48 bits of the A and Q Registers Z places in a right circular fashion with Q_0 shifted into A_{23} and A_0 shifted to Q_{23}.



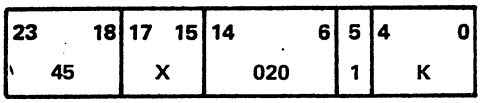
DRL - (Shift) Double Right Logical. DRL shifts all 48 bits of the A and Q Registers Z places to the right. A_0 is shifted into Q_{23}. Bits shifted out of Q_0 are lost. Zeros are shifted into A_{23}.



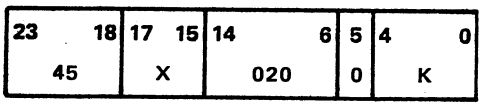
MAQ - Move A to Q. MAQ places the contents of the A Register into the Q Register. The original contents of Q are lost. Zeros are placed in the A Register.



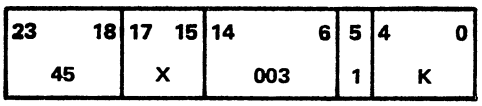
SLA - Shift Left Arithmetic. SLA shifts the contents of the A Register Z places to the left. Bits shifted out of A_{23} are lost. Zeros are shifted into A_0. The overflow flip-flop is set if any bit shifted into A_{23} is unlike the original content A_{23}.



SLL - Shift Left Logical. SLL shifts the contents of the A Register Z places to the left. Bits shifted out of A_{23} are lost. Zeros are shifted into A_0.



SLC - Shift Left Circular. SLC shifts the contents of the A Register K places to the left. Bits shifted out of A_{23} are shifted into A_0.



Quasi Instructions - Quasi commands provide operations not included in the hardware. They supply the programmer with a mnemonic which allows the running program to be linked to a subroutine. Quasi commands store the effective operand portion of the command (Z) in Index Register 2 and the next instruction is "fetched" from a memory location determined by the operation code (bits 23 through 18) of the Quasi command. The command located at the specified operation code address is normally an SPB which branches to a software subroutine associated with the Quasi command. The combination of the Quasi command storing the value Z in cell 2 and then executing the instruction in the operation code address completes the operation to be performed for these commands.

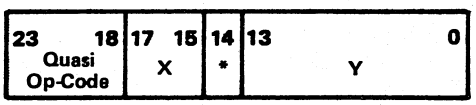
Although the function to be performed by the Quasi command depends on the instruction located in the related memory vector, certain operation codes are normally reserved to perform specific Quasi functions, thereby, providing program compatibility with other Honeywell computers. The following is a list of these commands:

Quasi Op-Code	Memory Vector	Use
22	42	Undefined
23	44	Undefined
43	43	Undefined
54	54	STM - Store Multiple
64	64	LDM - Load Multiple
70	60(DP)	FAD - Floating Add*
70	70(SP)	FAD - Floating Add*
71	61(DP)	FSU - Floating Subtract*
71	71(SP)	FSU - Floating Subtract*
72	62(DP)	FMP - Floating Multiply*
72	72(SP)	FMP - Floating Multiply*
73	63(DP)	FDV - Floating Divide*
73	73(SP)	FDV - Floating Divide*
74**	40(DP)	FIX - Fix Floating Point
74**	74(SP)	FIX - Fix Floating Point*
74**	41(DP)	FLO - Float Binary Point*
74**	75(SP)	FLO - Float Binary Point*
76	76	Reserved for RTMOS
77	77	Reserved for RTMOS

SP = Single Precision, DP = Double Precision

The Quasi instructions cannot be interrupted following execution. That is, the command located in the operation code address must be executed before an interrupt can occur. Instructions within the Quasi subroutine, however, may be interrupted following execution provided the instruction is normally interruptible following execution.

Commands that are located within the Quasi subroutine and not relative addressed are subject to the established protect criteria.



Z = f(X,*,Y)

*These become hardware commands if the Firmware Floating Point option is present.

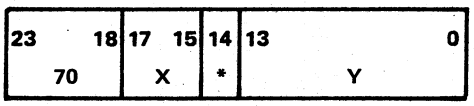
**Bits 12-14 are also decoded. Op-code 74 may be a FIX, FLO, or FMS.

Floating Point Hardware Instructions

The following commands (except FMS) are single instructions when the Firmware Floating Point option is present, otherwise they are Quasi instructions. Both will destroy the contents of Index Registers 1 and 2 and the J counter when executed.

FAD - Floating Point Addition. The normalized single (or double) precision floating point number in memory location Z (Z + 1) is added algebraically to the normalized floating point number contained in the A (or A, Q) Register. The sum is placed in the Arithmetic Unit A (or A, Q) Register in normalized floating point format. The contents of memory location Z are unchanged. If implemented as a Quasi, these instructions may not be the object of an OOM instruction.

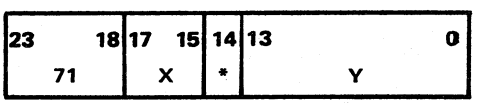
If an overflow occurs during the add operation, the overflow flip-flop is set and the "bad value" number 40000000_8 is placed in the A Register. If an underflow occurs during the add operation, the A Register is cleared (i.e., 00000000_8) to denote a standard zero result.



Z = f(X,*,Y)

FSU - Floating Point Subtract. The normalized single (or double) precision floating point number in memory location Z (or Z, Z + 1) is algebraically subtracted from the normalized floating point number contained in the A (or A, Q) Register. The normalized result is placed in the Arithmetic Unit A (or A, Q) Register in normalized floating point format. The contents of memory location Z are unchanged.

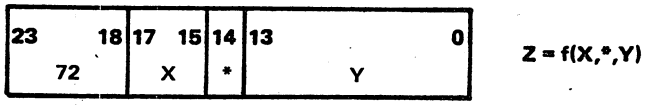
If an overflow occurs during the subtract operation the overflow indicator on the Programming and Maintenance Console is lighted and the "bad value" number, 40000000_8 is placed in the A Register. If an underflow occurs during the subtract operation, the A Register is cleared (i.e., 00000000_8) to denote a standard "zero" result.



Z = f(X,*,Y)

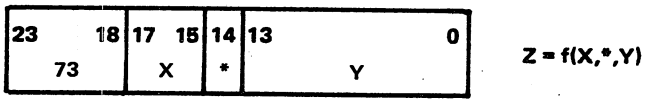
FMP - Floating Point Multiply. The single (or double) precision floating point number in the A Register (or A, Q) is multiplied by the normalized floating point number contained in memory location Z (or Z, Z + 1). The product is placed in the A Register (or A, Q) in a normalized floating point format. The contents of memory location Z are unchanged.

If an overflow occurs during the multiple operation, the overflow indicator on the Programming and Maintenance Console is lighted and the A Register is set to the "bad value" 40000000_8. If an underflow occurs during the multiply operation, the A Register is cleared to denote a standard zero result (i.e., 00000000_8).

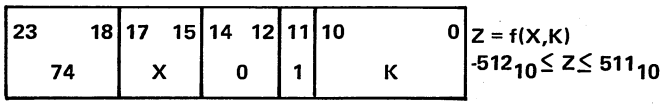


FDV - Floating Point Divide. The normalized single (or double) precision floating point number in memory location Z (or Z, Z + 1) is divided into the normalized floating point number in the Arithmetic Unit A (or A, Q) Register in normalized floating point format. The normalized quotient is placed in the A (or A, Q) Register. The contents of memory location Z are unchanged.

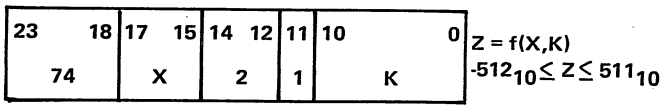
If an overflow occurs during the divide operation, the overflow flip-flop is set and the "bad value" 40000000_8 is placed in the A Register. If an underflow occurs during the divide operation, the A Register is cleared (i.e., 00000000) to denote a standard zero quotient.



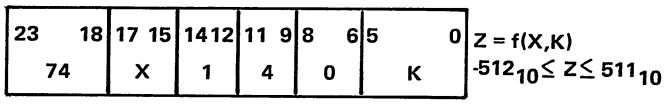
FIX - Fix Floating Number. FIX converts a single or double length floating point number contained in the (A) or (A, Q) Register, to a fixed point number in (A) or (A, Q) with the scale factor Z. The overlfow flip-flop is set if arithmetic overflow occurs. When in double precision mode, FIX is executed as a Quasi routine. In single precision mode, FIX may be executed by the firmware if that option is present.



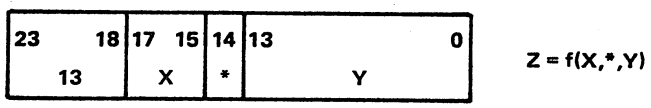
FLO - Float Fixed Number. FLO converts a fixed point number with the scale factor Z, contained in the (A) or (A, Q) Register, to a single or double length, normalized, floating point number. The overflow flip-flop is set if arithmetic overflow occurs (i.e., the magnitude of the exponent exceeds five bits). If arithmetic underflow occurs (i.e., the magnitude of the exponent exceeds five bits), the result is set to zero (00000000).



FMS - Floating Mode Shift. FMS sets and resets the single/double word indicator in bit 23 of the program counter. Bit 23 reset indicates single mode and bit 23 set indicates double word. If (Z) bit 0 is set the shift is to single word mode and if (Z) bit 0 is reset the shift is to double word mode.



BIB - Branch If Bad. Branch If Bad branches to memory location Z if the A Register contains an unnormalized floating point number.



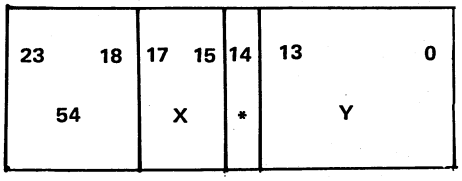
BIB becomes a NOP command if:

The A Register contains all zeros

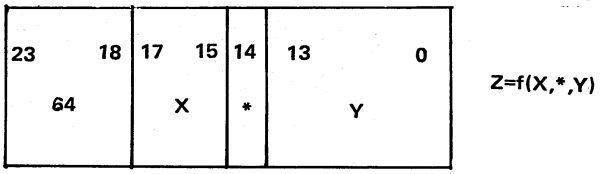
A Register bit 16 is set and the single precision F/P mode is selected

A Register bit 13 is set and the double precision F/P mode is selected.

Other Quasi: Instructions



STM - Store Multiple. STM is a quasi instruction that stores the contents of index registers 3 through 7 into memory locations Z through Z + 4. The contents of the A and Q registers are preserved. The contents of index register 2 are destroyed.



LDM - Load Multiple. LDM is a quasi instruction that loads index registers 3 through 7 with the contents of memory locations Z through Z + 4. The contents of index register 2 are destroyed.

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